# DIRC Digital Chip Preproduction Tests Results

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This report describes the tests results of the digital preproduction chip designed at LPNHE Universités Paris 6 et 7 for the DIRC detector of BaBar. Full description and specifications can be found in reference [1].

The chip has been manufactured by ES2 (Rousset, France), with the Cadence-ES2 design kit. 110 prototypes have been received in May 1997. They were previously successfully tested by the manufacturer using an 8k test-vector file provided by LPNHE in order to check the digital functions.

The first 10 prototypes were tested in standalone and then mounted on the DIRC Front End Board for further tests. Systematic tests were performed on the remaining 100 prototypes. Test procedure and results are described below. The full results are available on the web at: $http://www-lpnhep.in2p3.fr/babar/Hughes/tdc\_test.html$.

## 1 Test bench.

In order to test the chips, a 4 layer PCB card has been designed, with $16 \times 50\Omega$ time inputs, digital input/output ports and a readout sequencer allowing to digitize and read simultaneously, as well as to check the selective readout algorithm and the input capability (figure 1).

It is connected to the following instruments:

- 16 PMTs + LED,
- LeCroy 9210 fast pulser,
- IEEE488 I/O card,
- Philips PM5786 pulser as clock generator,
- Low voltage supplies.

The LeCroy pulser, the I/O card were under control of the LabView-3 (National Instruments) software, running on a MacIntosh Quadra computer. A test software has been written, allowing to input various stimuli and use several readout modes, with provision for interactive test, histograms displays, statistics, and diagnostics.

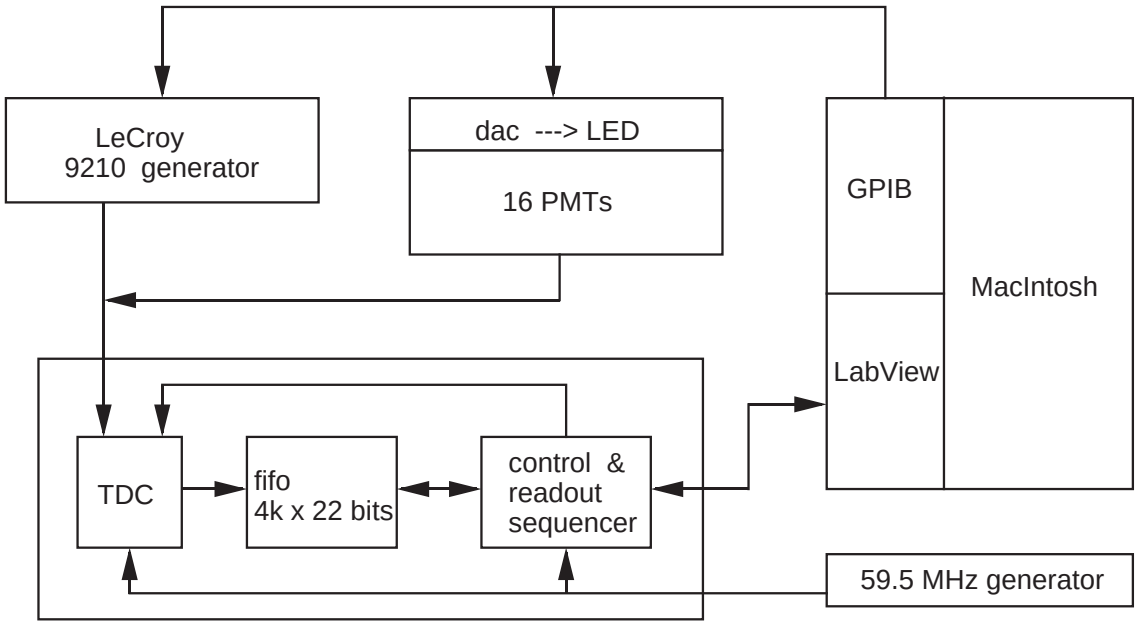


Figure 1: Test Bench.

# 2 Tests.

Ten tests were performed in order to check the basic functions, the selective readout and the linearity of the circuit.

## 2.1 Basic functions.

- Calibration working in the power supply range from 4.5 to 5.5$V$.
- Test of the input mask.
- Check that data were read each time an L1 trigger occured.

## 2.2 Linearity.

### 2.2.1 Monotony.

In order to check the linearity on the whole range of the TDC, two random signals in asynchronous mode with respect to the trigger (500 $kHz$) and with a fixed time difference were applied on all channels. The time difference was set 2 clock periods + 1 LSB of the TDC to check the continuity of the time response between the coarse and the fine chains. The test ran until about 90% of the

codes were measured at least once. The output time difference was measured. No entries out of a $\pm$ 2 LSB range around the nominal value were allowed.

If the test failed, the chip was calibrated on 31 bins instead of 32 by simply changing the calibration type bit and the test was performed again. The chip was rejected if the test failed with both types of calibration.

#### 2.2.2 Differential linearity.

Random signals were applied to the 16 inputs with an average frequency of 120 $kHz$ and the occupancy of the 32 bins was plotted for each channel. The rms on each channel was required to be smaller than 100 $ps$. In any case, the test was performed with the two types of calibration.

### 2.3 Selective Readout.

The following tests have been done with 12 $\mu s$ latency and 1 $\mu s$ resolution.

#### 2.3.1 Trigger count.

The 16 channels are pulsed synchronously with the trigger in the middle of the window with a readout frequency of 125 $kHz$. No loss should be observed over 1000 triggers.

#### 2.3.2 Readout time window.

In order to scan the full window, the 16 channels were pulsed asynchronously with the trigger (400 $kHz$ free running generator frequency, 1000 triggers). All hits should fall within the trigger window.

#### 2.3.3 Efficiency.

The efficiency was measured by applying random inputs on 15 channels (average frequency of 200 $kHz$) and one trigger synchronous pulse every 2 $\mu s$ on channel 0. A 100% efficiency was required after 1000 triggers.

#### 2.3.4 Status word generation.

In order to induce the 'FULL' status word generation, all channels were pulsed each 2050 $ns$ and the channel disabling limit was set to 4 $MHz$. Data losses should be correctly notified by the 'FULL' status word.

To check the channel disabling, the input rate period was set to 1700 $ns$ and the disabling limit successively to 4 $MHz$ and 500 $kHz$. The 'FULL' status word should be generated in the second case but not in the first case if 8 channels are pulsed at once.

# 3 Results.

## 3.1 Linearity.

Figure 2 shows the rms on each channel for all chips when the calibration is performed on 32 bins. A peak around 40 $ps$ is observed as well as a tail towards high values. The peak is due to typically channels 1 to 13 while the tail is usually populated by channels number 0, 14 and 15. The rather high rms observed on these channels is due to bin 31 being too large as shown on figure 4b.

If calibration is performed on 31 bins only (figure 3), the rms for channels 0, 14 and 15 gets smaller (around 45 $ps$) while the values of other channels increase to 80 $ps$ mainly because of bin 0 being too narrow (see figure 5a).

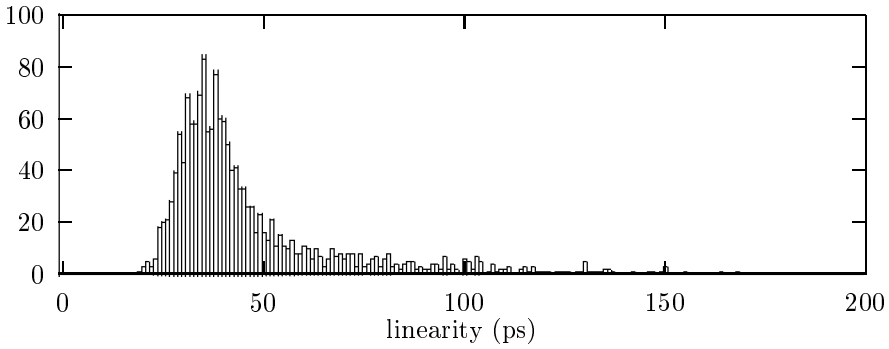


Figure 2: Differential linearity for all chips and all channels (calibration on 32 bins).

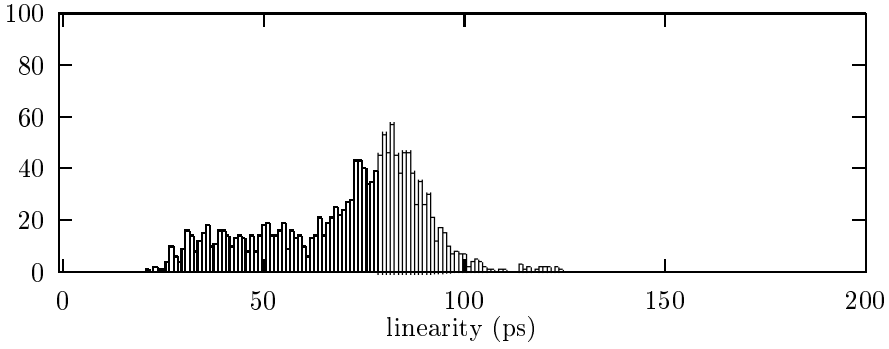


Figure 3: Differential linearity for all chips and all channels (calibration on 31 bins).

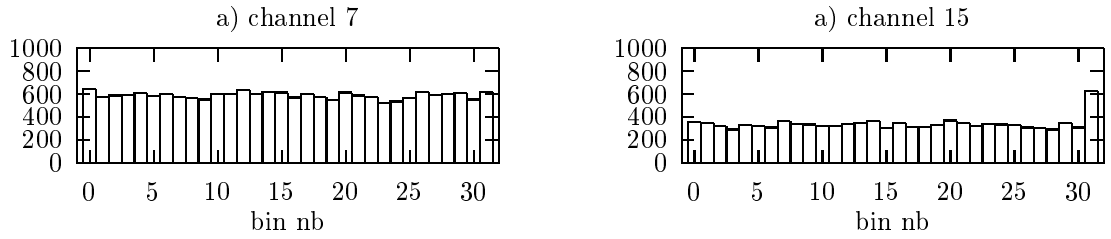


Figure 4: Number of hits per bin for one typical chip: a) channel 7, b) channel 15 (calibration on 32 bins).

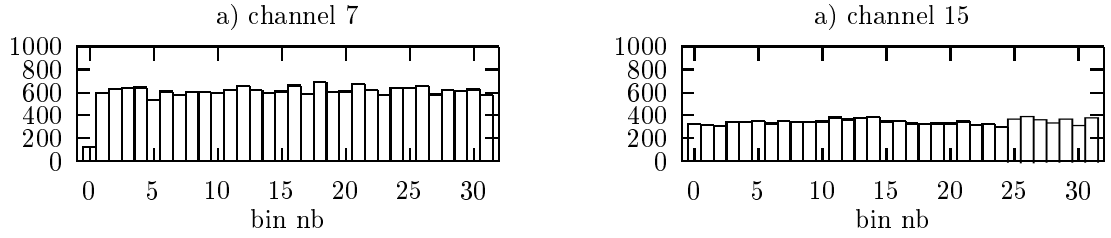


Figure 5: Number of hits per bin for one typical chip: a) channel 7, b) channel 15 (calibration on 31 bins).

### 3.2 Readout time window.

Scanning the readout time window, it was observed that hits were missing in the first 67.8 *ns* of the window and that extra data falling outside of the window were sometimes readout (figure 6).

Missing hits are due to L1 occuring exactly when a datum is transferred from the latency FIFO to the output FIFO. This was corrected by extending the window by 67.8 *ns* so that no useful data are lost. Extra data are recorded if L1 occurs while the output FIFO is being cleared. The extra amount of data due to these two effects is of the order of 10% in normal running conditions.

In order to take these effects into account, the test was validated if data fall within the range of bins 180 to 204.

### 3.3 General results.

Over 100 chips, 9 chips were rejected for the following reasons:

- bad readout window: 1 chip.
- hits outside the $\pm$ 2 LSB range in the monotony test: 1 chip.
- channels with linearity greater than 100 *ps*: 4 chips.

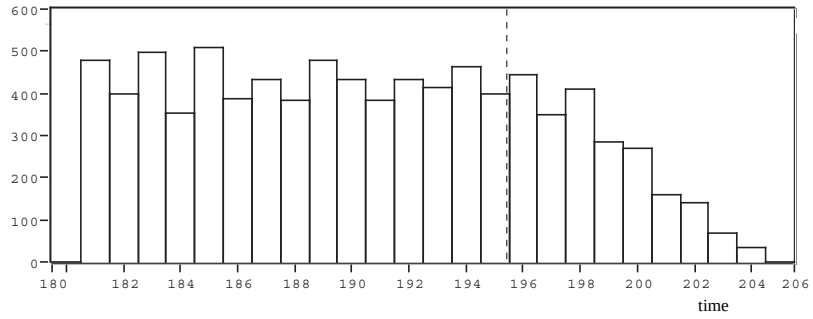


Figure 6: Number of hits as a function of time. The trigger window includes bins 180 to 195. Bin width is 67.8 $ns$.

- 1 chip failed both the channel disabling and the differential linearity test
- 2 chips failed all the selective readout and the linearity tests.

38 chips were validated with calibration on 32 bins and 53 chips required calibration on 31 bins for validation.

# 4 Conclusion.

100 prototype chips were fully tested on an automatic test bench at LPNHE. Defect observed on trigger window was easily corrected by changing the window by 67.8 $ns$. Extra amount of data is of the order of 10 %.

No major problem was observed. A 91 % yield was measured. The production of 1250 pieces started in June 1997. The chips are expected end of September.

# References

[1] Philippe Bailly, Jacques Chauveau, Jean-Francois Genat, Hervé Lebbolo, Zhang Bo. The DIRC Digital Chip Reference, June 2d 1997.