Nuclear Science Symposium
&
Medical Imaging Conference

October 22d-29th 2011, Valencia, Spain

Short report

Jean-Francois Genat
LPNHE Paris

NSS-MIC 2011

- 2100 participants
- 1700 contributions
  - 600 orals
  - 1100 posters
- 370 Students
- 100 sessions in 8 days !

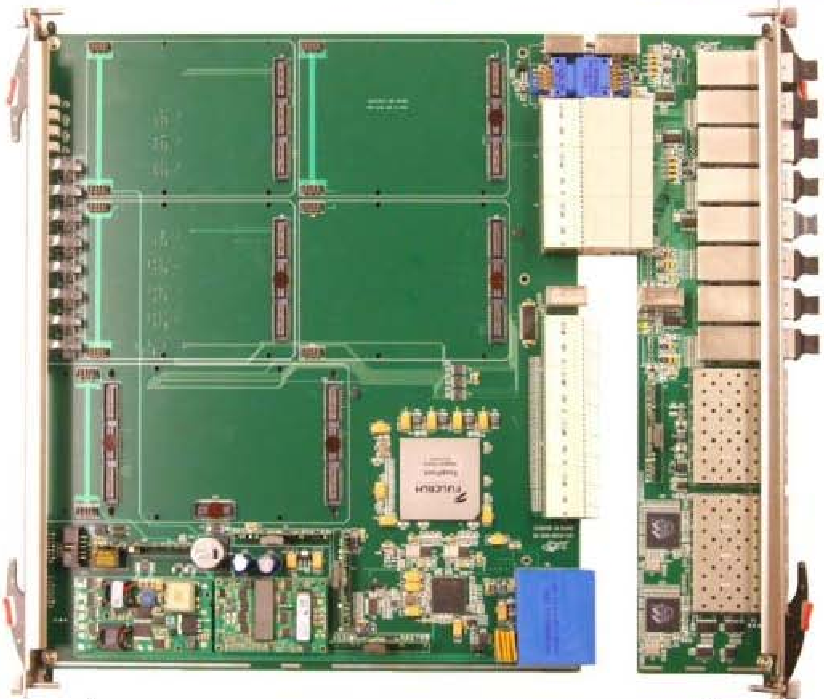
David W. Townsend, General Chair
National University of Singapore

5th *Workshop on ATCA and MicroTCA for Physics*

Venue: Hotel Melià Valencia Palacio de Congreso

Dates: October 22-23, 2011

Information: http://www.nss-mic.org/2011/NSSMain.asp



ATCA PICMG 3.8 New RTM Standard

MicroTCA MTCA.4 New IO RTM Crate & Modules

2011 IEEE Nuclear Science Symposium and Medical Imaging Conference

Workshop On Room-Temperature Semiconductor X-Ray And Gamma-Ray Detectors

23-29 October 2011, Valencia, Spain

Short Course Program

An excellent set of short courses will be given at the start of the NSS/MIC programs, covering a wide range of nuclear and medical imaging technology. All courses are one day in length. The first lecture will begin at 09:30. Lunch, refreshments, lecture notes, and a certification of completion are also provided as part of the short course registration fee.

Contact:

Joao Varela
NSS Short Course Chair

Grant Gullberg
MIC Short Course Chair

Course Name	Date
1. Experimental Techniques in Nuclear and Particle Physics	Sat. Oct. 22
2. High-Precision Calorimetry for Particle and Nuclear Physics Experiments	Sat. Oct. 22
3. Integrated Circuits for Time and Amplitude Measurement of Nuclear Radiation Pulses	Sun. Oct. 23
4. MStatistical Approaches to Tomographic Reconstruction	Sun. Oct. 23
5. Kinetic Modeling	Sun. Oct. 23
6. Statistical Approaches to Medical Image Analysis	Mon. Oct. 24
7. Physics and Design of Detectors for SPECT and PET	Mon. Oct. 24

Nuclear Science Symposium 2011

Detection components

- Scintillators
- Photodetectors
- Solid state hybrid and monolithic detectors
- Gaseous detectors

Front End, DAQ, Trigger electronics

- Analog and digital circuits
- Low noise highly integrated front end electronics
- Digitization and signal processing
- DAQ architectures and hardware standards
- Multi-level trigger approaches and trigger farms
- Fault tolerance and radiation hardness

Software and Computing

- Core software tools
- Simulation and analysis
- Distributed and grid computing

Detectors/Intrumentation (small systems)

- Gamma-ray and neutron detection
- Nuclear detectors
- Tools and techniques for bio-medical research
- Synchrotron radiation and accelerator instrumentation
- Homeland security

Large detection systems

- High energy physics and nuclear physics detectors
- Astrophysics and space instrumentation

Invited Lectures

- Tribute to J. A. Rubio (Accelerators in Spain)
- Lessons from Fukushima

Outline

- Crystals
- Silicon PMs
- Other Fast photo-detectors
- Pixels
- Low noise
- Analog signal processing
- Timing, TDCs, Fast serial links
- FPGAs
- Triggers and DAQ, new standards

Crystals

Light yield - Energy resolution / Speed trade-off

G. Gundiah LBL
B. W. Sturm LLNL

Ternary Halogenides

Meng et al, Journal of Rare Earths, 2006, 24, 503

http://scintillator.lbl.gov

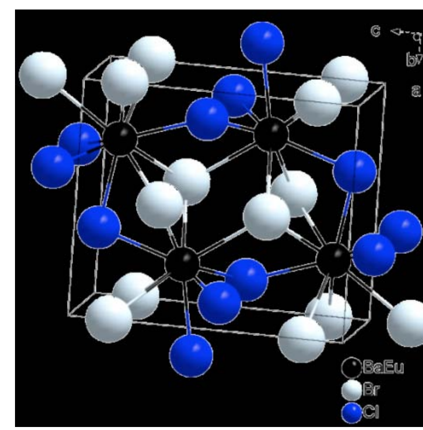
SrI_2(Eu)

80,000 ph/MeV, 100ns-1μs decay

BaBrCl: 5-8% Eu2+

56,000 ph/MeV, 550ns

3.6% at 662 keV



BaBrCl

Crystals

Light yield / Energy resolution / Speed trade-off

B. J. Connors , Georgia Tech

ZnO Neutron Detectors (High Sensitivity and Gamma-Ray Discrimination)

Picosecond time constants (not shown)

Wilkinson, J., K. B. Ucer, et al. Radiation Measurements **38(4-6): pp501-50**

S. R. Tornga, Los Alamos

Compton Camera (Balloon boarded, γ astro 0.4-20 MeV)

Combination of **$LaBr_3$** absorbing and custom organic scattering detectors: 12.000 photons

$\delta E / E$ =11%, 210ps ($LaBr_3$), angular resolution 6°

Crystals

Light yield / Energy resolution / Speed trade-off

V. Nagarkar, Radiation Monitoring Devices, USA

- γ ray imaging
- LaBr3:Ce
- Yield 73,720 photons $\delta E / \sqrt{E}$ 7% at 122 keV and ~4.7% at 662 keV for spectroscopy
- Space resolution 140μm for SPEC

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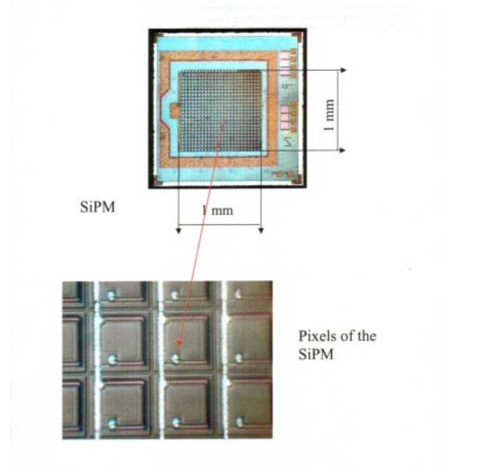
Silicon PMs (SPADs, Geiger APD, MPPC…)



Geiger multiplication in Silicon

Reverse biased PN junction (50-70V)

- Pixels
- Gain 10^6
- QE 90% reduced by filling factor (quenching resistor takes space)
- Spectral response of Silicon (visible)
- Use of a standard ''cheap'' CMOS process
- Readout can be integrated
- Timing resolution <100ps
- Very low gain fluctuations
  single/multiple PE resolution

Drawbacks

- VERY noisy (MHz/mm^2)
- Crosstalk (optical)
- Fill factor (see later)

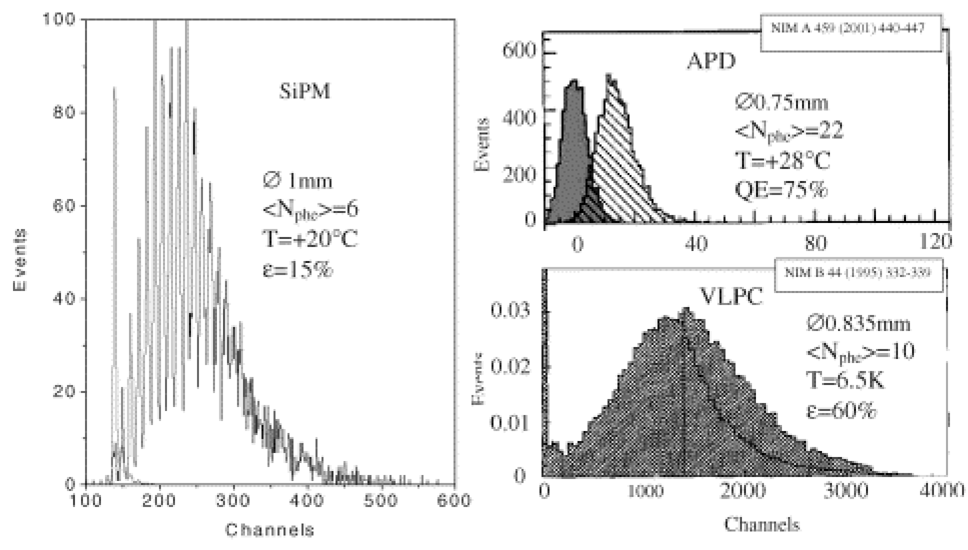


Fig. 3. SiPM application for sci fiber MIP detection (at room temperature): comparison with APD [6] (room temperature) and VLPC [7] (6.5°K).

Silicon PMs

- Model of Detectors for PET applications
  A.C. Therrien, U Sherbrooke

- Highly integrated arrays of digital SiPMs with easy readout interface
  C. Degenhardt, PHILIPS

- Study of coincidence time resolution for various scintillators of different size and wrappings read out by SiPMs using the time over threshold method
  E. Auffrey, CERN

- New Photosensors and scintillators for fast timing applications
  L.M. Fraile, U Madrid

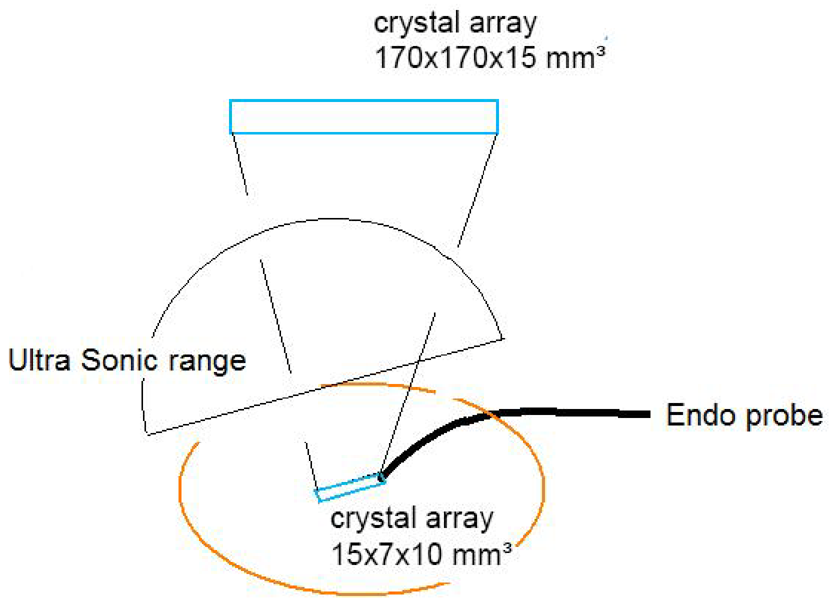
Silicon PMs

- Single Channel Optimization for an Endoscopic TOF PET Detector
  C. Xu, DESY

- A dual modality PET/UltraSound endoscopic probe to develop new biomarkers of pancreatic and prostate cancers

  Technical challenges:
  - Excellent TOF resolution O(200ps)
  - O(1mm) space resolution = excellent granularity

Silicon PMs



Endoscopic probe
160 – 320 single channels
Crystal: 0.75x0.75x10 mm3
Readout using SiPMs array with integrated digital circuit (TU Delft)

External PET plate
4k single channels
Readout using conventional SiPM

Custom designed chip for high time resolution performance,
ASIC prototype submitted. (U. Heidelberg)

Silicon PMs

Timing performance of large area SiPMs coupled to LYSO with noise compensation methods

C. Piemonte, FBK Trento

Time-of-Flight capability of FBK (Trento) SiPMs

couples a "slow" scintillators (e.g. LYSO)

Main concerns for large area SiPMs:

fill factor, high dark noise, signal shape, capacitance…

Method integrated in an ASIC, reduce the effect of dark noise on timing performance.

Silicon PMs

Difference between rise time and fall time: baseline fluctuations are removed

Identical initial part of the gamma signal, use the leading edge on the differential signal

- **Medium and high SiPM over-voltage**:

Gain increases

LED starts flat (increase of signal is compensated by the increase of noise)

DLED improves following signal

Timing resolution FWHM: 190ps (RT) 165ps -20°C

Silicon PMs

SiPMs with bulk integrated resistors

J. Ninkovic MPI

Advances in fill factor: Integration of the biasing resistor in Silicon bulk

Benefits:

- no polysilicon
- larger fill factor
- less optical cross talk

Drawbacks:

- Constraint on the wafer thickness
- vertical ‘resistor‘ is a JFET: longer recovery times

130nm 20μm pitch Fill factor >70%, Crosstalk 15%

Digital Silicon PMs

Model and Measurements

Herman T. van Dam, TU Delft

Provide number of photons and Time of arrival

4 x 4 dies, 2 x 2 pixels, 6400 cells

- Single photon per cell
- No analog electronics
- Each cell can be enabled/disabled individually:
- Noisy cells can be switched off

Digital Silicon PMs

- Trigger on one cell above threshold, start TDC stopped by system clock,
- Wait 45ns for more than 4 photons above threshold, reset if no
- Read all die (800ns)

- Non-linear correlation between energy and number of fired cells

Measurements:

- 3x3x5 mm^3 LSO:Ce,Ca crystals

- Total dark count rate:
- 2.9 x 2.9 mm^2 pixel : $2.5 \cdot 10^6$ Hz
- 3800 cells enabled only: $5.1 \cdot 10^2$ kHz

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- Pixels
- Low noise
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- Timing, TDCs, Fast serial links
- FPGAs
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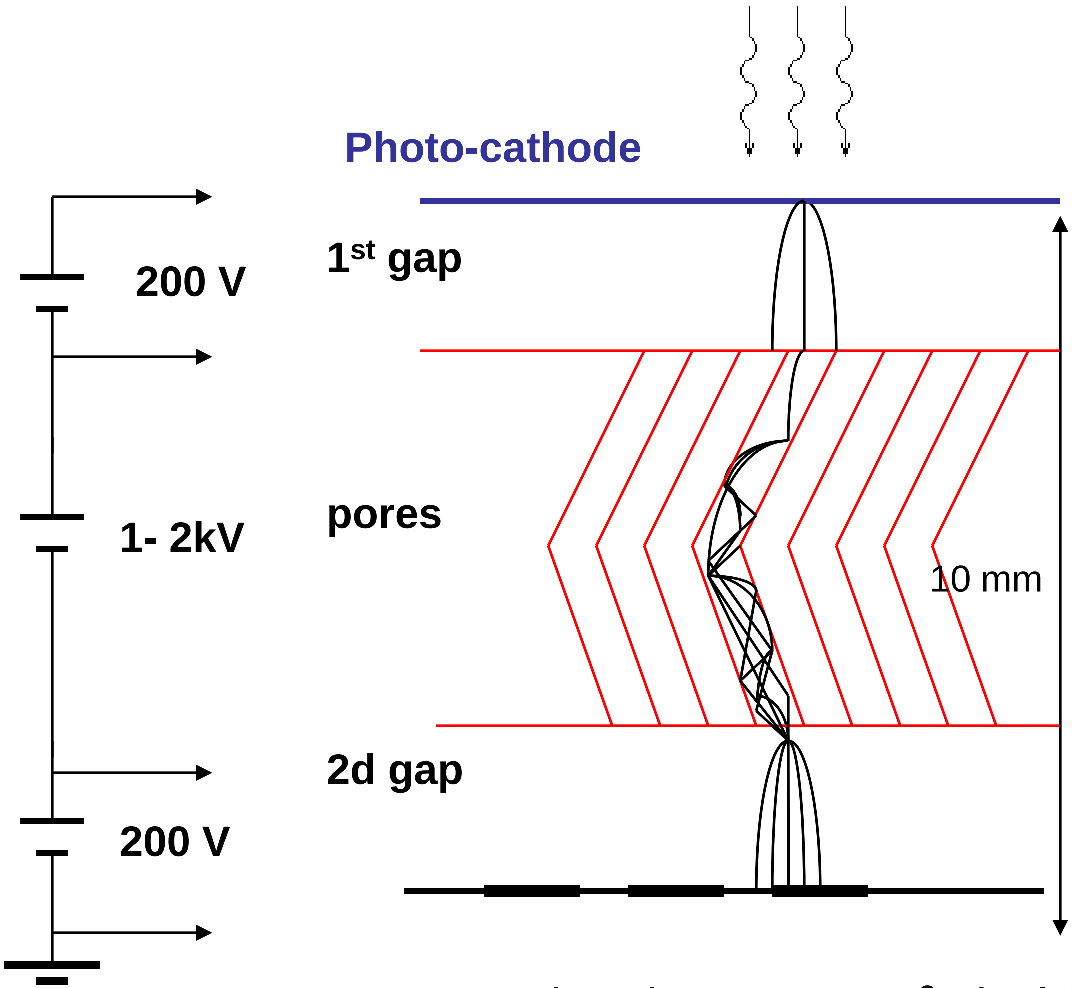
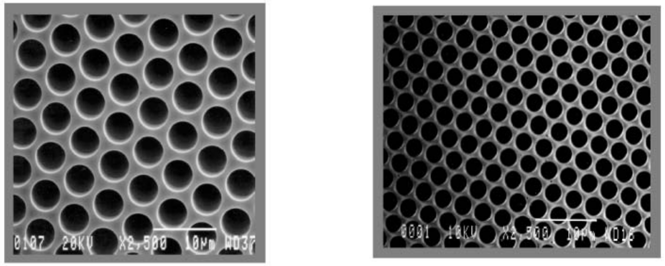
Micro-Channel Plate Detectors



Anodes (1.6 x 1.6mm^2 pixels)

Pore diameter: a few µm



Comparison of 5micron pore and 2 micron pore MCP's (same magnification)

Pore diameter 3-25 µm
Pore aspect ratio: 1:50
Radiation hard

Micro-Channel Plate detectors

Development of Large Area Photon Counting Detectors Optimized for Cherenkov Light Imaging with High Temporal and sub-mm Spatial Resolution

O. Siegmund
SSL Berkeley

Large Area Picosecond Photodetector Program (DOE)

- Argonne National Lab.,
- U. Chicago,
- UC Berkeley and several other National Labs

Universities and Industry develop large area (20cm) sealed tube sensors with optical photo-cathodes and novel microchannel plates for high speed timing/imaging applications in HEP, RICH, Astronomy, etc.

Large Area Picosecond Photodetector Program (DOE)

40µm pore, 60:1 L/d, Atomic Layer Deposition MCP pair

First 20cm MCP ALD imaging without any opportunity for optimization.

Background still very low.
Timing resolution < 50ps
Spatial resolution is ~100µm FHWM
Mean gain ~4 x 10^6

- ALD functionalized MCPs: borosilicate glass microcapillary arrays made in 33mm and 20cm at 20µm and 40µm pores and 8° bias.

- Performance characteristics similar to standard commercial MCPs both in analog and photon counting modes.
- MCP preconditioning: very good gain, outgas and stability.
- 20cm, 40/20µm pore MCPs: normal gain behavior.
- Background rates low, <0.1 events cm^{-2} sec^{-1}.
- Design and fabrication of 20cm sealed tube
- Semitransparent Bialkali (25%) cathodes on glass

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Pixels

ATLAS pixels
C. Lange DESY

3 barrel layers, 2 end caps of 3 disks, 80 Mchannels
Radiation hardness: 500 kGy / 1015 1 MeV neq cm-2
T=-13°C

Sensor:

- 250 µm n-on-n 16.4×60.8 mm2
- 47232 (328 x 144) pixels
- Typical pixel size 50 x 400 µm2
- bias 150 to 600 V

Read-out:

- 16 FEI3 250nm chips, bump-bonded to 2880 pixels-
- zero suppression in the FE chip
- ToT
- data transfer 40 -160 MHz (optical)

-- timing spread 170ps

Status:

0.1% disconnected bumps
>0.04% analog dead, 10% merged bumps
>96.8% of pixel detector operational

Pixels Radiation damage

- increase of leakage current
- increase of full depletion voltage
- decrease in charge collection efficiency
- increase already measurable on all layers at module level

B-layer R&D

S. Grindstein IFAE Barcelona

Insertable, remove actual (hard failures)
Better radiation hardness, faster and larger FEI4 chip 130nm

200 um Planar and 3D pixels (CNM FBK)
>97%) after irradiation (5E15 neq/cm2) achieved

RD50

A. Rummler

Expect $2 \cdot 10^{16}$ neq cm-2 for pixels at HL-LHC

Pixels

Radiation tests for planar and 3D

Dose: 1.4.1016 neq cm-2

Planar n in n:
97% CCE at 1800V

3D: High charge (15 ke-) measured after HL-LHC fluence
70% CCE at 425V

Pixels

Fast, Radiation Hard, Direct Detection CMOS Imagers for High Resolution Transmission Electron Microscopy
B. Krieger, LBNL

CMOS direct detector

- Higher PSF and DQE
- High-speed
- High-resolution
- 6MPix, 6.4 Gp/s
- 100 Mrad tol
- 21 x 22 mm2
- 16 Mpixel, 400 frames/s, camera based on the imager commercialized

Next:

400 x 400 prototype in standard 65 nm CMOS
2.5 µm pixel pitch

Pixels

Large Area Ultra-Thin Detector Ladders based on CMOS Monolithic Pixel Sensors
W. Dulinski, IPHC

Sparse readout sensor for EUDET beam telescope
> 2 cm^2 active area, 0.7 Mpixel tracker
Readout: 100 µm integration →10 kFrame/s)
Space resolution < 4 µm for a pitch 18.4 µm
MIP eff. > 99.5 %
Fake hit rate < 10^{-6}
Radiation hardness > 10^{13} n/cm^2 (high resistivity epi substrate)

Ultimate: 4 cm^2 sensor for STAR Microvertex upgrade
Radiation hardness >10^{14} n/cm^2 with CMOS MAPS

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Low Power 12-bit ADC for a Liquid Argon TPC

N. Nambiar, BNL

DUSEL:

TPC 70 tons. -200 m South Dakota

Long Baseline Neutrino Experiments (LBNE)

ADC: 12 bit 2MHz, 3.6 mW, no steady clock, sleep mode, RT and 77K

0.6mm^2, 180nm CMOS

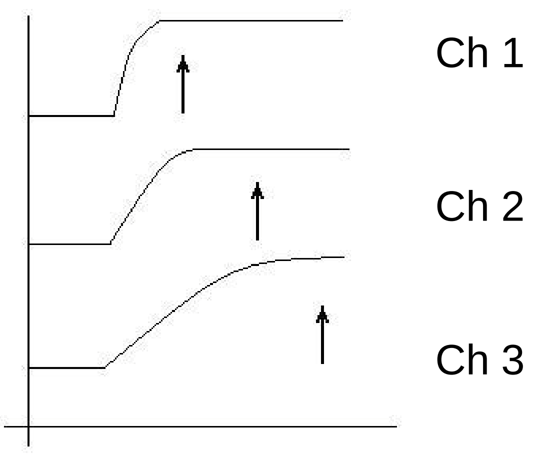
- Successive approximations by comparison and subtraction of the encoded result using current sources
- Provision for transient suppression
- INL/DNL < 1.5%, 11.6 bit ENOB

Multiplexed Oversampling Digitizer in 65 nm CMOS for Column Parallel CCD readout

C. Grace LBNL

1000 columns, no room for on detector amplifier: readout ASIC

Digitization scheme:



Save power with shaper bw reduction

ADC: Pipelined 12 bit 80 MHz (J.-P. Walder)
1 ADC/ 4 channels
0.35 mm^2 / ADC
30 mW/ADC
Measured noise: 0.8LSB,
INL/DNL 10 bit
65 nm TSMC (Design kit available from MOSIS)

PARISROC, An Autonomous Front-end ASIC For Triggerless Acquisition in Next Generation Neutrino Experiments

F. Dulucq LAL

PMm2: "Square Meter Photomultiplier" (2007-2010):

Innovative electronics for photo-detectors

Replace large PMTs (20-inch) by macro pixel (2*2 m²) of 16 smaller ones (12-inch) with central ASIC :

- Trigger less front-end electronics with independent channels at 65 m underwater
- Charge and time measurement
- Common HV
- One wire out (DATA + power supply) to the surface DAQ

PARISROC 2 : AMS SiGe 350nm

- 16 channels, 17 mm^2
- Single channel rate: 5 kHz
- Charge dynamic range: 1- 600 p.e. (100 pC)
- Resolution: 0.2 pe (32 fC)
- Disc threshold: 0.3 pe (50 fC)
- Timing resolution: 170 ps
- Timing precision < 1 ns

NECTAr0, New High Speed Digitizer ASIC for the Cherenkov Telescope Array

E. Delagnes, Saclay

2 Channels

Memory 1024 Cells

Power Consumption	210
Sampling Freq. Range	0.5 - 3.2 GS/s
Analogue Bandwidth	400 MHz
Read Out deadtime	2 µs
Deadtime @ 10 kHz trigger rate	<2%
ADC LSB	0.5 mV
Total noise	< 0.8 mV rms
Maximum signal	2 V
Dynamic Range	>11.3 bits
Crosstalk	0.4 %
Relative non linearity (integral)	<3%
Sampling Jitter	< 40ps

Embedded Real Time Digital Signal Processing Unit for a 64-Channel PET Detector Module in a TSMC 0.18 µm CMOS ASIC

HL. Arpin, U Sherbrooke

Intended for PET CT with sub-mm resolution

New LYSO crystal and APDs

- TOT measurement, with optimized threshold value
- On-chip digital signal processing.
- Corrections for non linearity
- Event detection

Sequenced by a 100 MHz state machine

Implementation of Constant Fraction Discriminators in Sub-micron CMOS Technologies

S. Garbolino INFN Torino

- Optimization for silicon sensors
  - Dynamic range: 1fC - 10fC Collection time: 3ns, pixel area: 300mm x 300mm
  - First prototype for NA62 experiment:
    - Jitter @ 1MIP: 90ps (rms)
    - Time-walk resolution: 92ps (rms)
    - Power consumption: 840mW/channel
    - CFD area: 154mm x 74mm
    - 130nm process
- Next:
  - Improve layout for jitter
- Decouple delay and fraction, higher order RC

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Constraints for sLHC
J. Kaplon (CERN)

ENC below 1000e-

Higher granularity and number of channels (order of magnitude)→

- detector capacitances 5 to 10 pF
- low power <300uW/channel

- Peaking time <25ns
- Stability → phase margin from 85 to 90 degree
- Reasonable PSRR
- Radiation hardness – doses >2×10^{14} N/cm^2 (1MeV) and >10MRad CMOS preferred

Excess noise in 90nm wrt 130nm,   1/f noise as well

Noise parameters do not scale short channel effects might caused excess noise for some technologies in 90 nm

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Deep Submicron CMOS technologies
M. Manghisoni (Pavia)

65 nm leakage current:

65 nm transistors are in the same region of current density values as 90 nm well below the commonly used limit of 1 A/cm2
CMOS scaling beyond 100 nm does not lead to very leaky LP devices

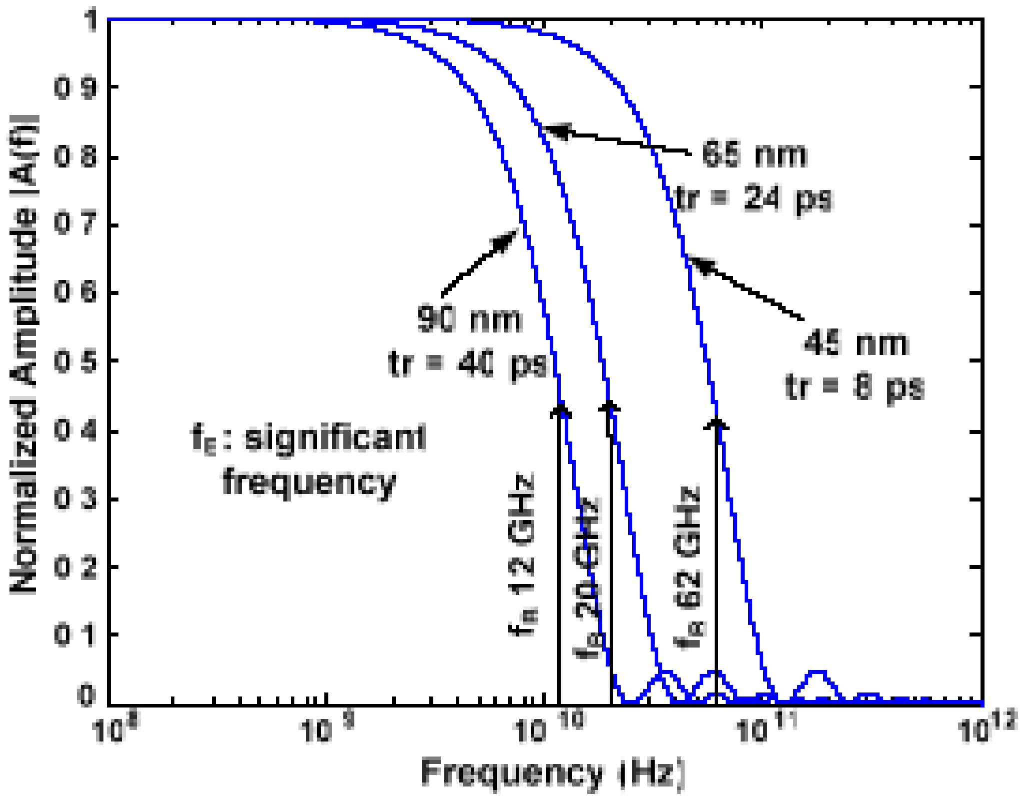
65 nm noise

No sizable short channel effects

Kf (1/f) parameter does not change going thinner
White noise: devices are biased close to weak inversion) white noise is not sizably affected by L and CMOS node variations even at minimum gate lengths

65 nm node: low-noise analog design, appears to be still viable

CMOS ICs Technologies



CMOS bandwidths from 90 to 45 nm technology nodes (ITRS 2005)

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A Multi-Channel, 10ps Resolution, FPGA-Based TDC with 300MS/s Throughput for Open-Source PET Applications

L.H. Menninga TU Delft

- Implementation of an Time-to-Digital Converter in an Virtex VI FPGA.
- Delay chain of buffers and D-flip flops
- Characterization of the performance of an FPGA-based TDC, wrt
  clock distribution,
  positioning,
  chip-to-chip variation,
  voltage and temperature,
  fluctuation, mismatches, calibration and parallelism.
- Optimization according to the characterization, nearing ASIC performance.

1 Gbit/S Serial Data Link Using Multi-Level Signaling for fast Readout Front-end or 3D-IC Applications

H. Mathez, IPNL

R&D for s-LHC (CMS tracker upgrade)

- Process : IBM 8RF DM 130 nm
- Chip size : 1 mm2
- Power consumption : ~ 40 mW
- First results up to 100 MHz
- Proof of concept
- Next

  Tests at full speed (250 MHz)

  Bit Error Rate measurement

  Improve ADC characteristics

  Add a tuning block to match DAC and ADC

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An acquisition system for CMOS imagers with a genuine 10 Gbit/s bandwidth

C. Guérin IPNL

- Open architecture (analog and digital CMOS imagers)
- On-line analog and digital processing
- Correlated Double Sampling, frame reconstruction, Kalmann filter, clustering
- High data rate
- No dead time
- Electron-Bombarded CMOS image (M. Winter IPHC)
- 10 µm pitch
- 3 transitors circuitry – external CDS needed
- 800 x 800 pixels – 4 sub-matrices
- 16 analog outputs
- 3 possible readout modes
- 40 MHz pixel clock-
- after 12bits/pixel digitization => 7.68 Gbit/s output data rate

- 2ms for in-line image computation
- Flash component to store FPGA Firmwares
- MAX II used to save Firmware via JTAG (Programming Flash Loader IP)
- At power up MAX II reads firmware from Flash component and configures FPGAs

Next

SW

- GPU computing

HW

- More on-board processing (Cluster finding, local noise suppression, …)
- Read several CMOS in parallel (Vertex tracking)
- 10 Gbit/s Ethernet with optical link (longer connection)
- True 40 Gbit/s Ethernet link

And much more !

THANKS !