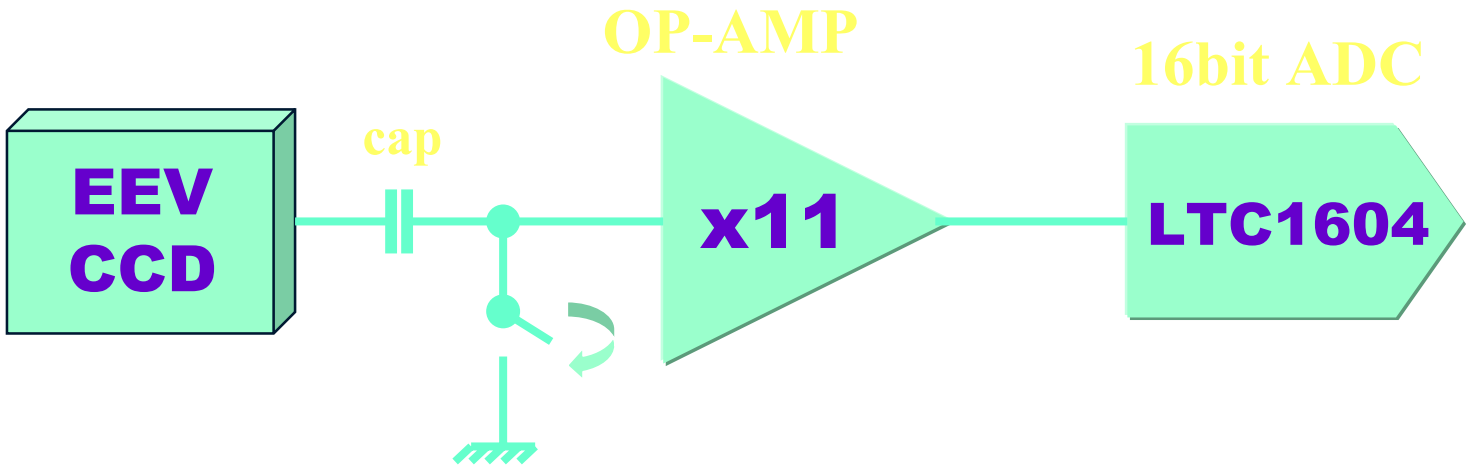
MEGACAM CLAMP & SAMPLE



BANDWIDTH : 1Mhz

- NOISE : 4e-
- PIXEL RATE : 200 Khz
- DYNAMICS : 14.5 bit

Our modifications

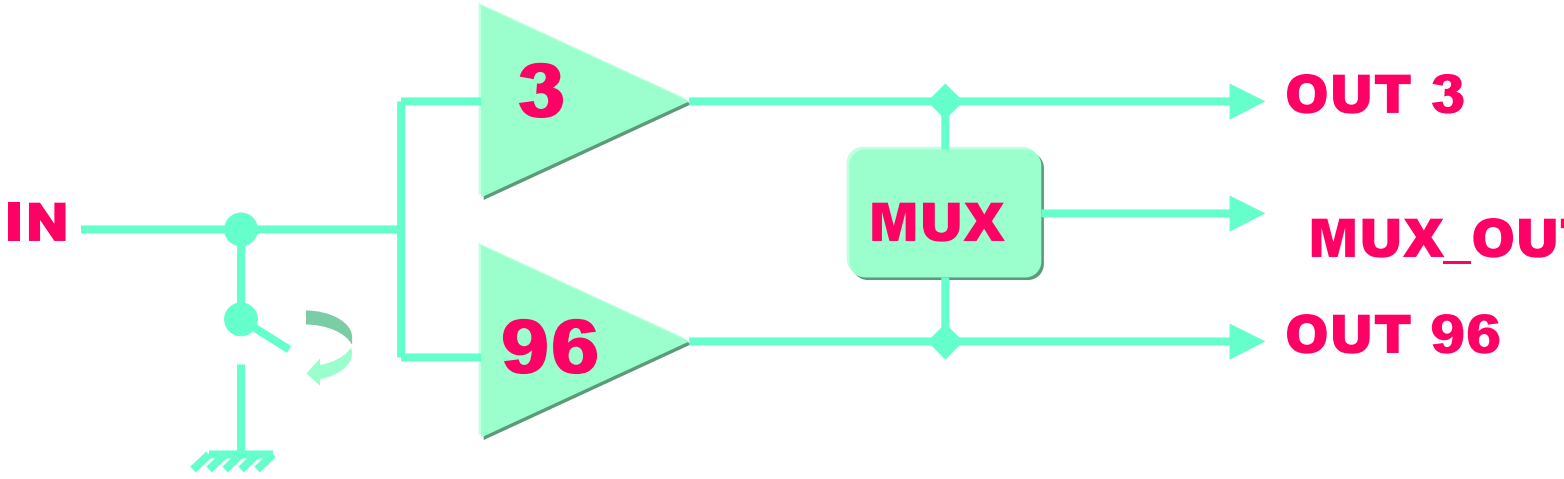
Proposed improvements :

- Increase dynamics with a double gain amplifier (17 bits)
- Optimize filtering to minimize noise
- Add an internal 12-bit ADC

How to validate the new system :

- *No coupling between high and low gain*
- *No 1/f noise limit up to 10kHz*
- *High stability of DC restore (≈CDS)*

LPNHE C&S ASIC



- Technology : CMOS 0.35µ AMS
- 4 Channels per chip
- Consumption : 1.5 mW
- Submitted : august 2003
- Received : November 2003

ASIC Problems

- Gain error : 60 instead of 96
- Offset error : -600mV on high gain

➢ Errors are due to bad layout drawing and are completely understood and reproduced in simulation.

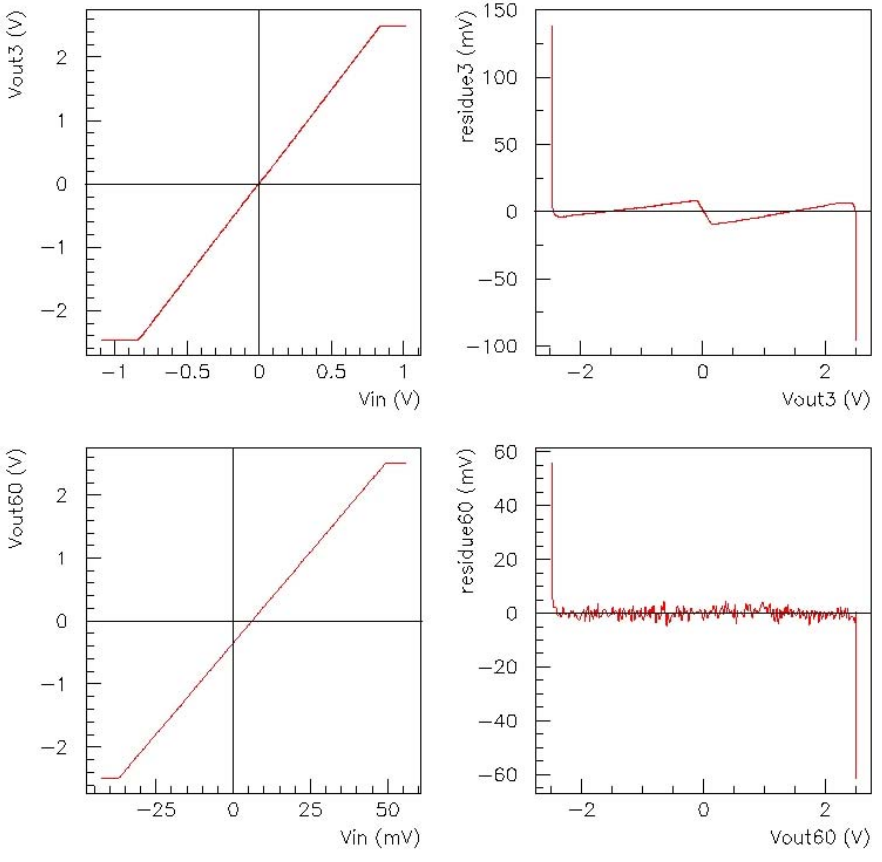
➢ A widespread problem : the design program for this technology does not take parasitic resistances into account.

C&S ASIC readout chain

- LabView framegrabber
- 2 x 16 bits ADCs per video card
- Rate $\leq$ 500 kHz
- CCD-like pulse generator (20bit DAC)
- A 1RG-clock card (UCSD for CCD clocks)

status: commissioning in course

First application: linearity check



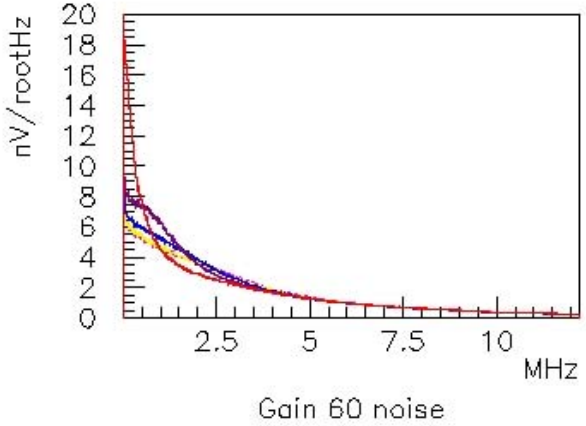
Readout&calibration chain assembled on Friday, May 14th

- Very good linearity for gain 60 output ; break in linearity for gain 3

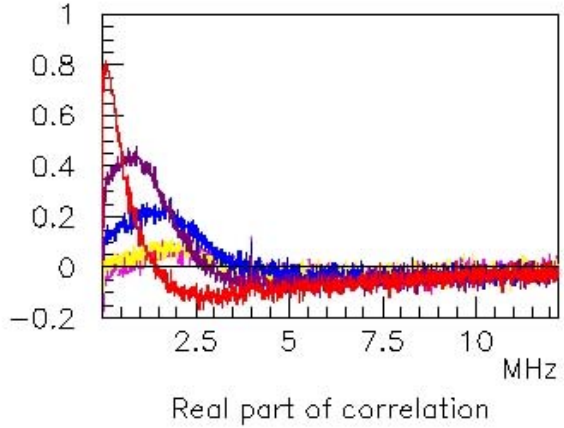
To be seen …

Digital signal analysis 1-

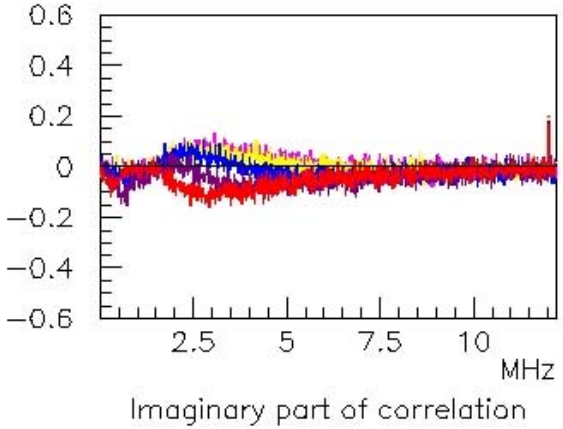
- coupled channel analysis → noise OK at percent level
- no undue correlation between gain 3 and gain 96



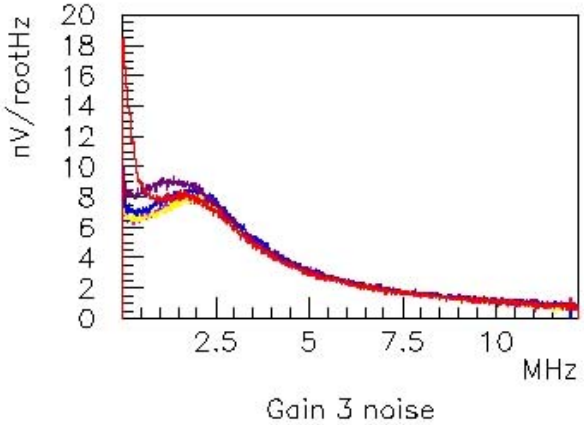
Gain 60 noise



Real part of correlation



Imaginary part of correlation



Gain 3 noise

R_{in} (emulates CCD R_{out})

- 20 kΩ
- 2 kΩ *
- 500 Ω **
- 50 Ω
- clamp

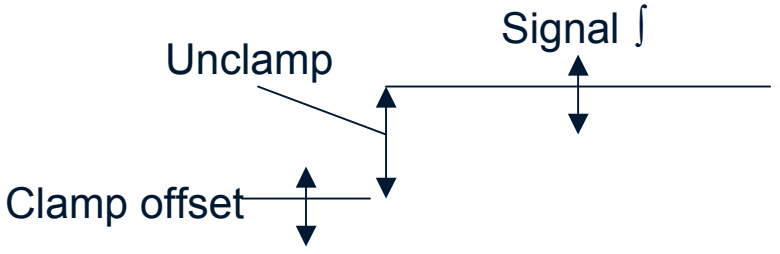
* LBL

**EEV

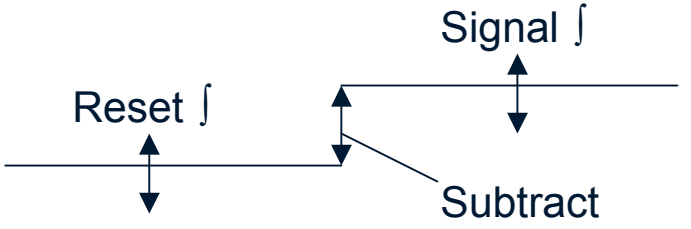
Digital signal analysis 2-

- Numerical filtering of ASIC digitized data
  → experimental measure of noise sources:
  1- affecting the clamp&sample mode
  2- affecting an ideal dual slope integrator
  using the same amplifiers

$$\sigma_{noise} = \sqrt{a^2 + b^2 \frac{T_0}{T} \eta(T)}$$



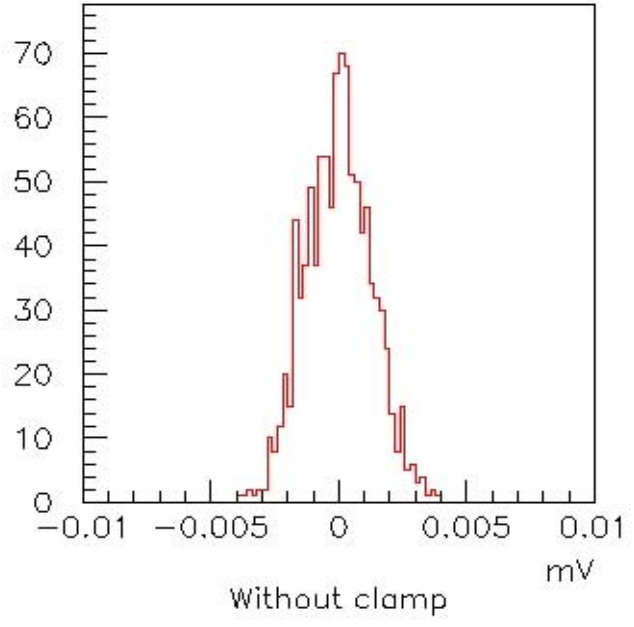
clamp and sample

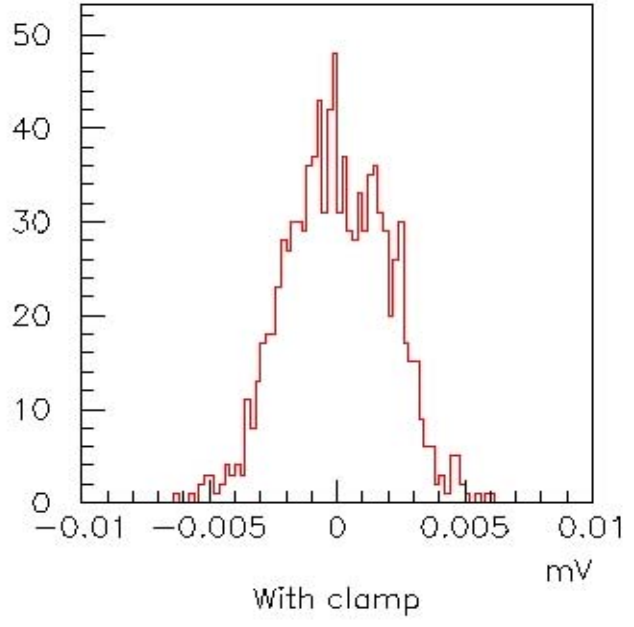


dual slope integrator

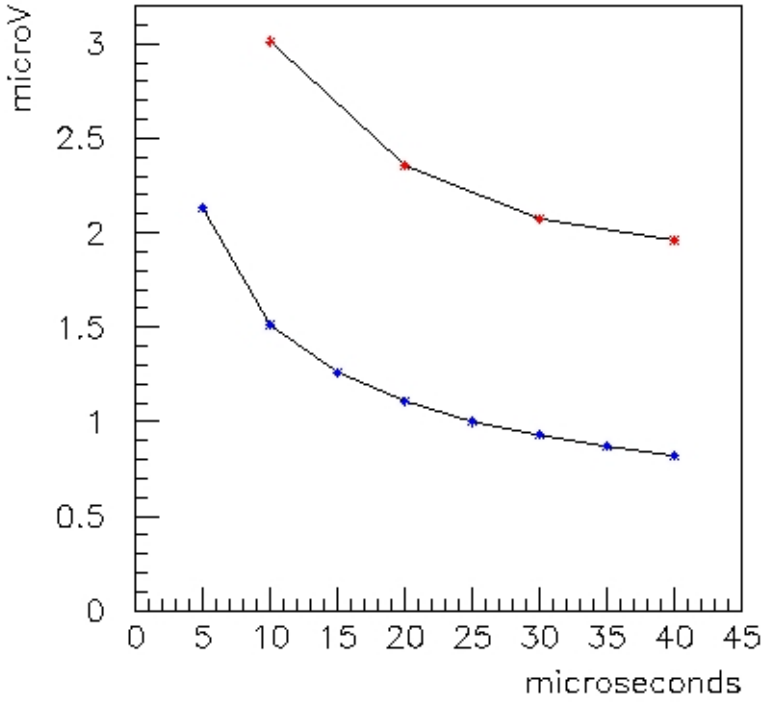
Digital signal analysis 3-

- Constant term a≅1.4μV due to unclamp (KTC) determined from RMS of 2 histograms (quadratic difference)





Digital signal analysis 3-



Time dependent part of noise of high gain amplifier with 2kΩ input

- Red: CDS mode
- Blue: Clamp&Sample mode

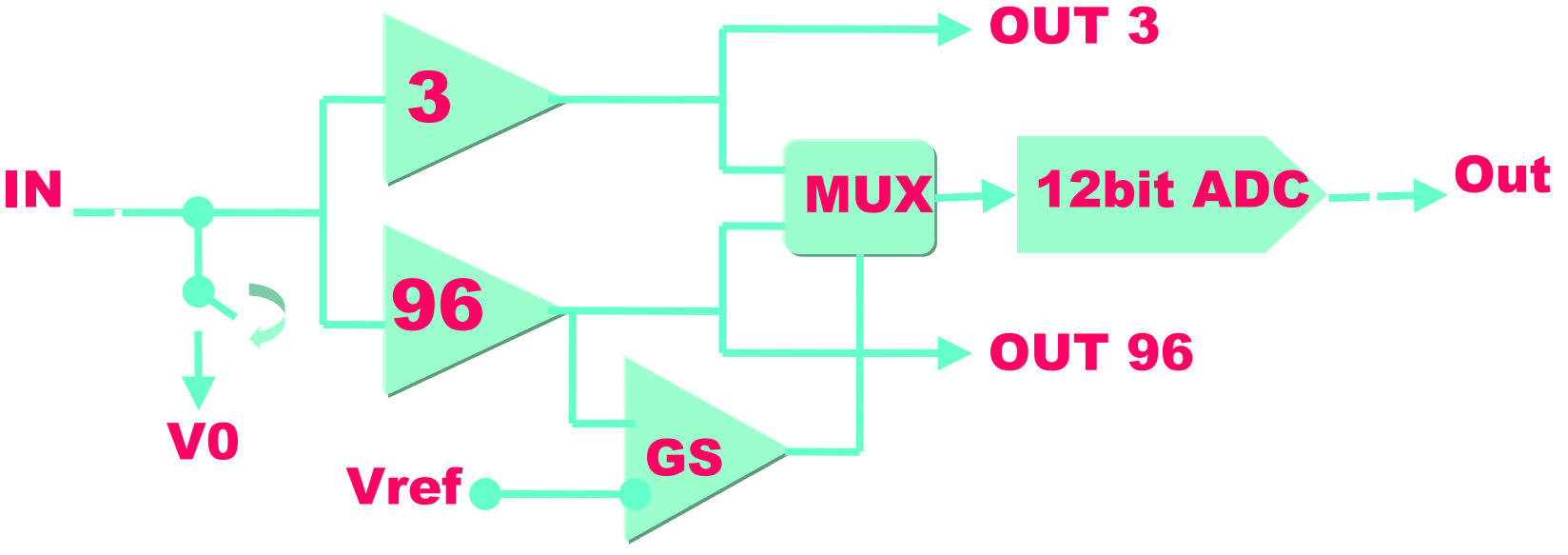
Time variable = total time for processing one pixel in µs

Amplitude = RMS in µV (conventionally take 1 e^- =4µV)

Other tests

- Irradiation test planned (@Dapnia)
- Full readout tests (June to December)
  -CCD readout in&out cryostat (140K)
  -Rockwell 1RG chain in IR cryostat
  (parameter extraction already done ≥ -20°C)

NEXT STEPS



- Integration of AMS analog cell 12 bit ADC
- Automatic gain select