SNAP CDS Test Chip: Midyear Summary

http://www-lpnhep.in2p3.fr/~barrelet/cds_test_04.pdf

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1 General

The CDS is made of two parts:

- the input amplifier PGA (Programmable Gain Amplifier)
- the integrating amplifier INT (Integrator)

Both parts can be disconnected and thus studied independently.

The experimental tests of PGA and INT are over[1]. They have been restricted by the small stability domain of both amplifiers.

Stability problems are mainly “large signal” ones, while simulation studies have essentially covered the “small signal” domain[2]. Understanding better the chip behavior would depend now on being able to simulate a large number of “large signal” configurations. We look for ward to having a complete installation in Paris of the full CDS ELDO simulator[3].

A good example of many test figures to be made in the large signal domain can be found in the data sheets of most commercial operational amps. This could be an inspiration for designing a CDS test package reproducing the problems found with our chip, in order to qualify a chip more completely at the simulation level.

2 Large Signal Domain

2.1 slew rates

The first relevant figure for the large signal domain are the slew rate figures: “slew rise” and “slew fall”. Figure 1 shows slew rates as a function of the capacitance applied on the output pads of the PGA.

This capacitance is used to stabilize the PGA. Above 100 pF all gain configurations are stable with PGA alone. The only stable configuration when INT is connected to PGA is gain 0.5 with 330 pF capacitors on each PGA output and each INT input.

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[1] personal opinion
[2] in our CDS small signal means very small, i.e. input signal below 1mV
[3] This is now done!

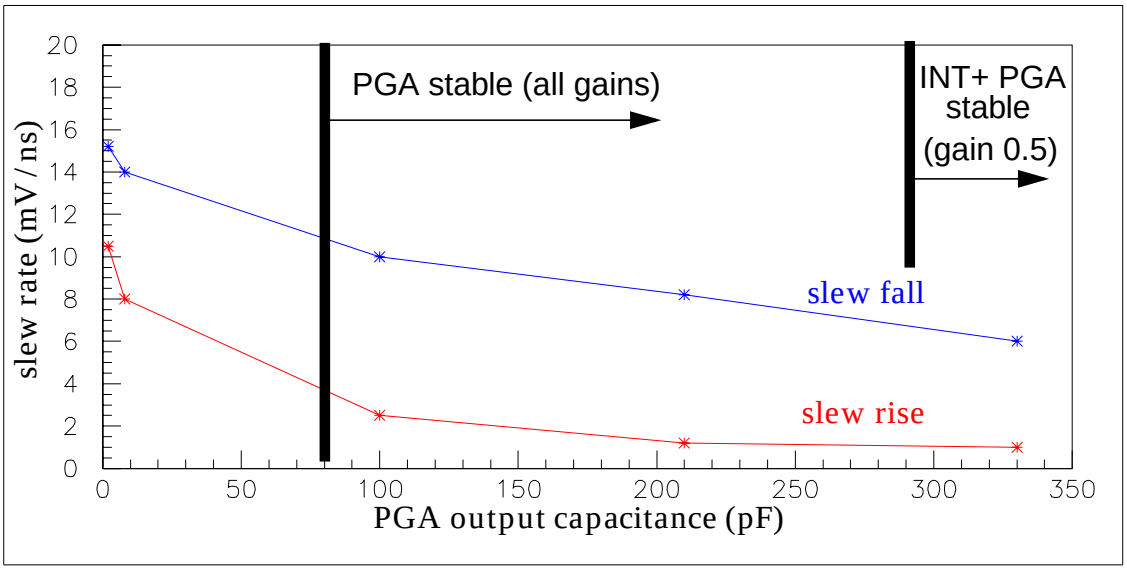

Figure 1: Slew rates of PGA as a function of output capacitance. This capacitance is used to stabilize both amplifier.

The PGA slew rates have two origins:

- the PGA output capacitors mentioned above which are either filled by a 0.25 mA current source or drained to ground when the PGA output transistor (follower) is either closed or open. Their effect is seen on Figure 1 above 50 pF.
- the 15 pF capacitors at the input of the same transistors which are either filled by the PGA gain stage (cascade) or emptied by a 0.2 mA current source. Their effect is seen on Figure 1 below 10 pF.

Usually the difference between slew rise and slew fall is kept below ±5%.

On this CDS chip rise and fall slew rates differ so much that large signals generate essentially a common mode output instead of a differential one.

2.2 common mode feed-back

Small signals generate very little common mode output because of the symmetric structure of the differential amplifier which is the core of PGA, but as seen above large signals generate a lot of it.

A unique common mode restoration mechanism is implemented in the CDS chip, using a feed-back loop shown in Figure 2 a). The common mode voltage reference V_{ref}= 3.4 V is provided by a dividing bridge inside the chip. The average of the positive and the negative PGA output $V_{\pm}=(V_{+}+V_{-})/2$ is provided by another bridge. The difference CMFB= $V_{\pm}$-V_{ref} is made by the differential amplifier C, and reinjected with a negative sign into the PGA input. This loop has been analysed with ELDO simulator. The loop was artificially opened by introducing a gap between the points CM and FB. The Figure 2 b) shows the variation of PGA output $V_{\pm}$ and the common mode error function CM as a function of the feed-back voltage FB applied.

This analysis shows a open loop gain for common mode feed-back of 3000 and a linearity domain very small (±150µV).

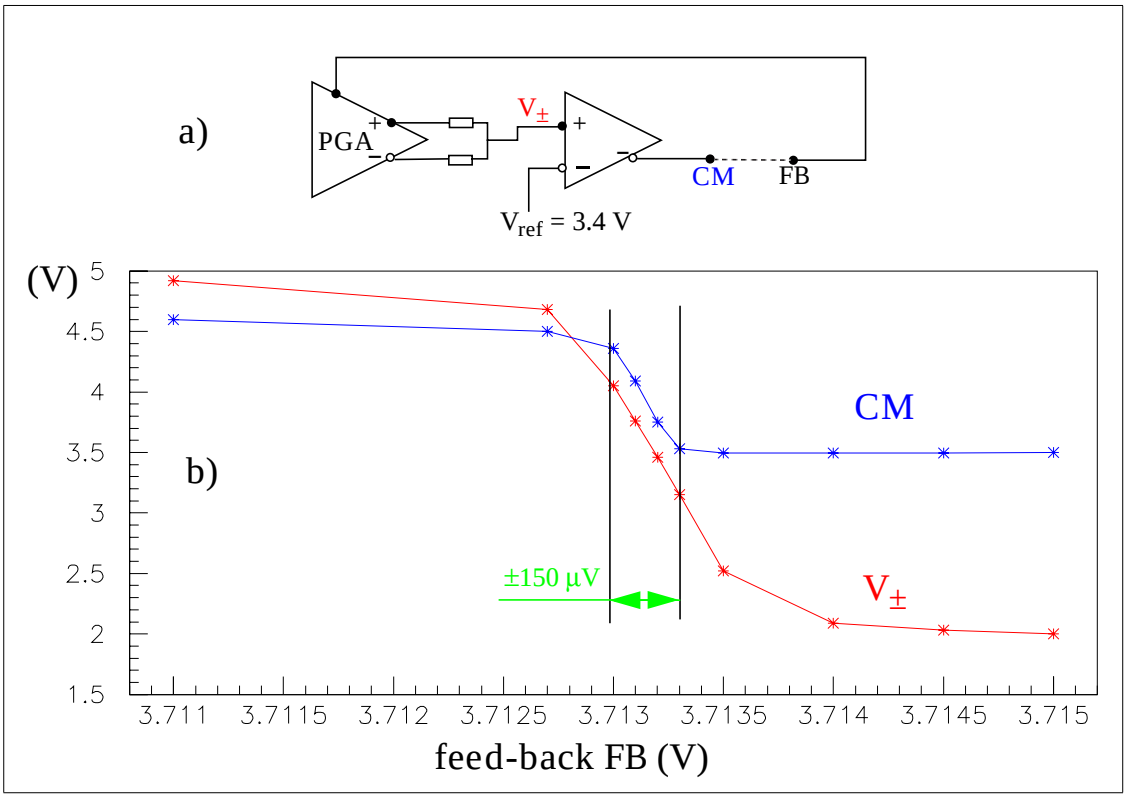

Figure 2: Open loop analysis of common mode feed-back (ELDO simulation)
a) the loop is broken between CM and FB; b) CM vs. FB curve in DC analysis.

2.3 saw-tooth instability

Because of the high open loop gain and the rise / fall asymmetry, the response of CDS to a step input yields sharp saw-tooth transients corresponding to an eternalness of the four states $(\text{fall}/\text{rise})_+ x\ (\text{fall}/\text{rise})_-$ which for a set of amplitudes of the step input gives rise to an unending oscillation. As an example of this behavior, let us show Figure 3 taken from a previous report[2]. Another example taken from an ELDO simulation is found in Figure 4. Here the oscillation is a pure common mode oscillation (the + and - outputs are rigorously the same). One can check that no transistor of the PGA works in a linear mode!

All transient and oscillation problems discovered so far seem to be due to these saw-tooth instabilities. They are seen as well in the PGA as in the INT behavior, as well at high and low frequencies (according to the capacitances involved). They are triggered by input signal and also by other CDS switches.

Short transients don't affect the stability, but they affect the quality of the CDS analog processing.

Saw-tooth instability seems also to cause the global instability of the whole CDS assembly, as seen in the next Section 2.4.

2.4 instability of the whole CDS (PGA+INT)

We have an experimental indication on the mechanism of CDS instability when operating PGA+INT at a critical gain (g=1). As seen in Figure 5, the PGA oscillates during its reset.

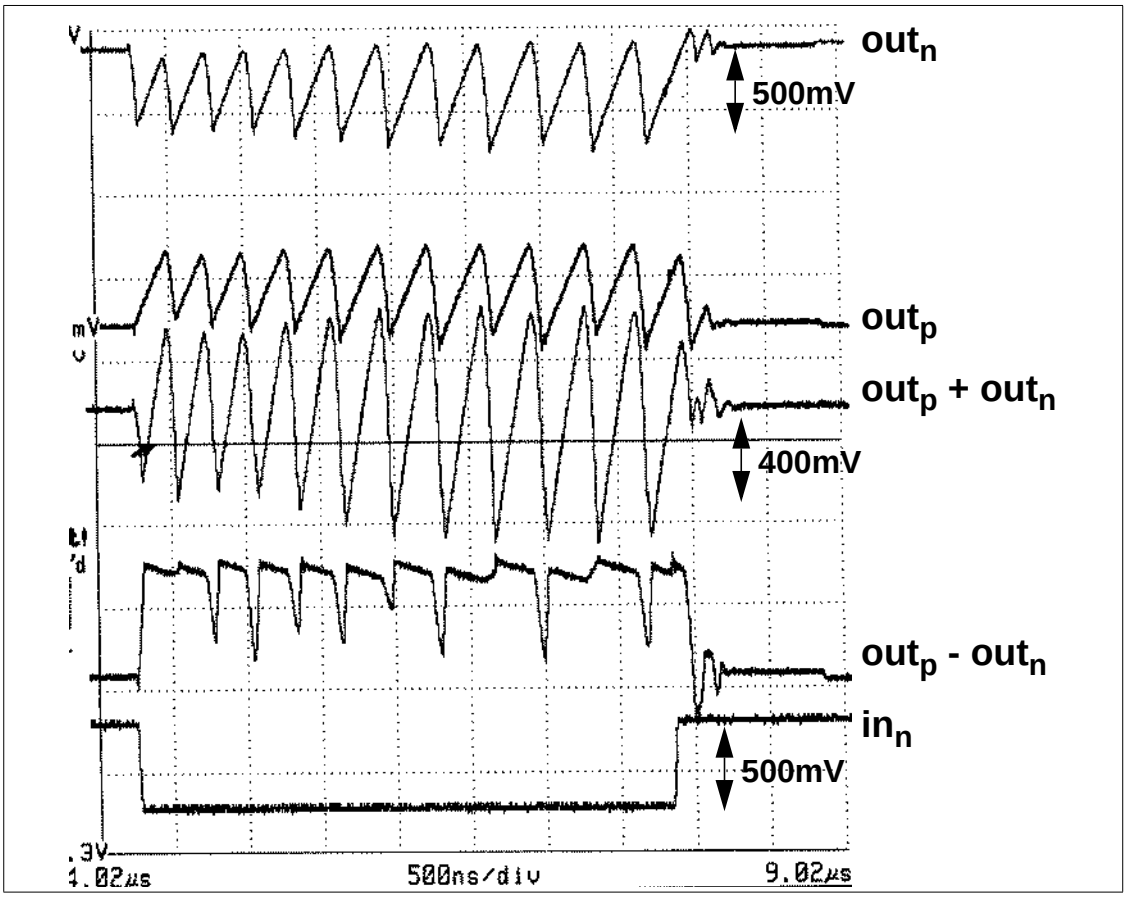

Figure 3: Saw-tooth common mode oscillation around a step function (experimental data cf. [2])

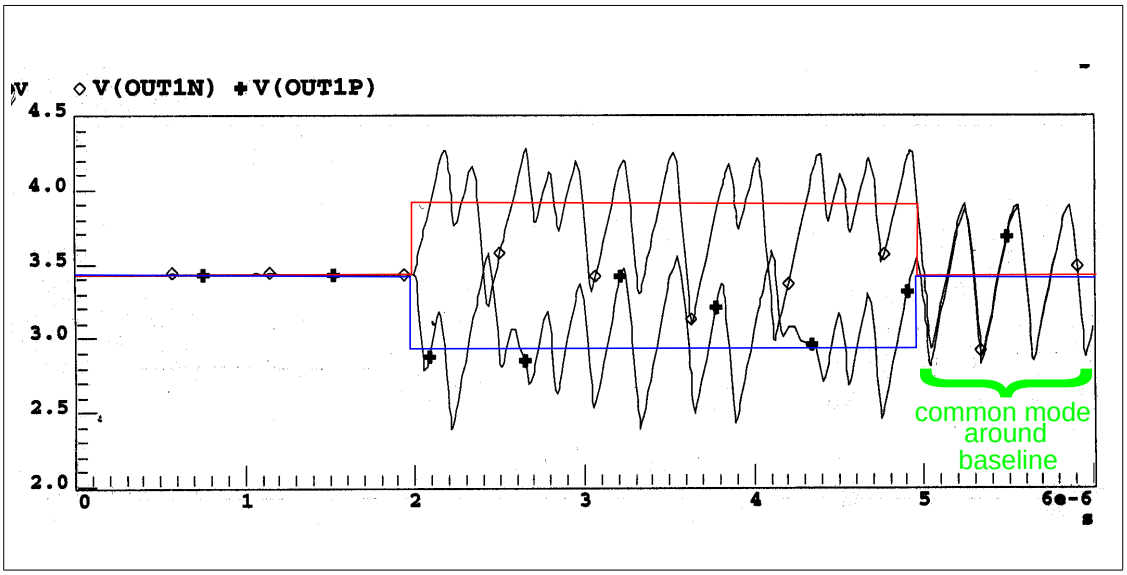

Figure 4: Saw-tooth common mode oscillation around the baseline (ELDO simulation). Here, as in Figure 3 the oscillation is triggered by a large signal.

This must be due to a conjunction of two effects: the saw-tooth instability and the over-constraint of the PGA reset mentioned in our previous report[2] (the over-constraint

means that there two competing feed-back loops). A full explanation, using the ELDO simulator, is still needed.

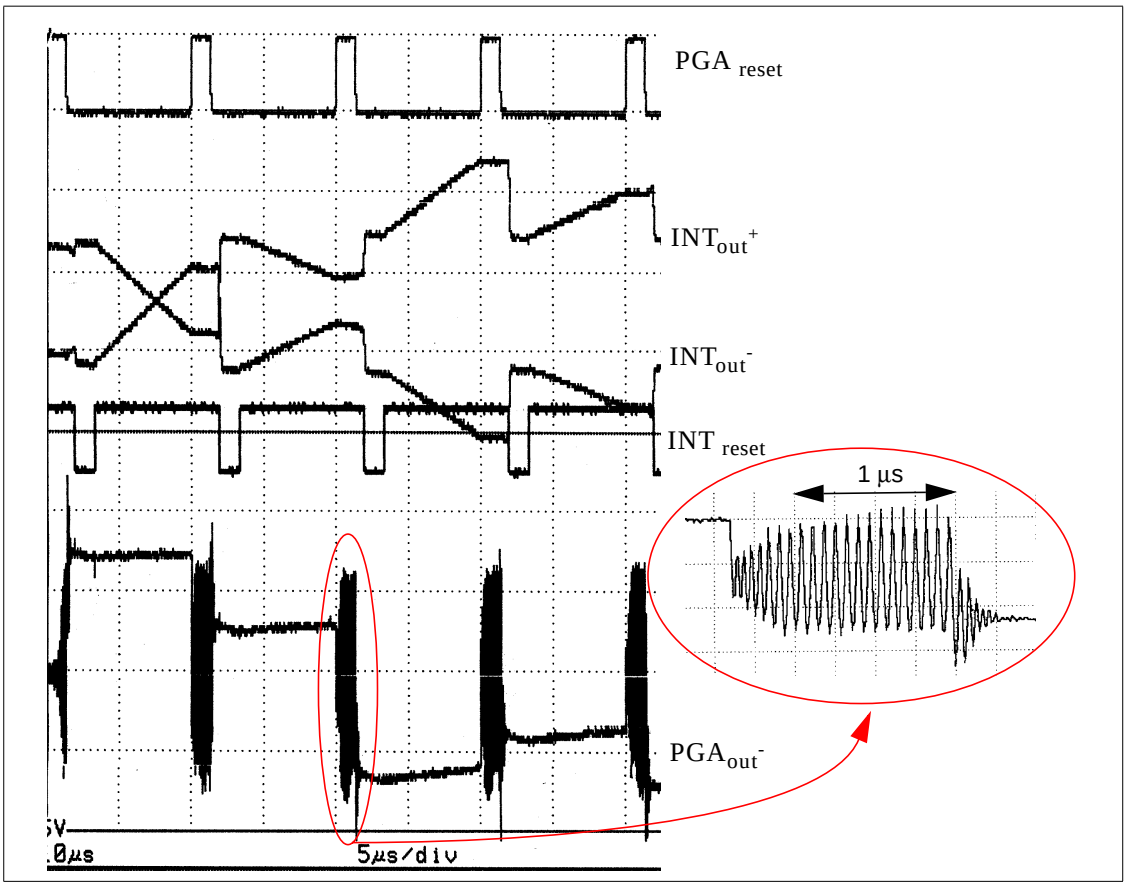

Figure 5: Onset of CDS instability: saw-tooth oscillation at 15 Mhz during PGA reset (experimental)

The result of this combination of effects is that, at the end of PGA reset, the baseline is frozen at an arbitrary value depending of the precise phase of the saw-tooth oscillation at the trailing edge of the reset.

Apparently the whole system -power-supplies included- breaks down when this baseline-less behavior is established.

3 Small Signal Domain

3.1 differential and common-mode noise spectra

A first report[1] has described the digital signal processing method used for baseline subtraction using the 1 Sample/s Tektronix digitizer.

The noise figures given in this report concern single CDS outputs. Jean-François Genat has argued that the significant figures are the differential noise and common mode noise.

We have therefore digitized both CDS outputs and made a baseline subtracted noise spectrum of the sum and the difference of the two CDS output which are shown in Figure 6.

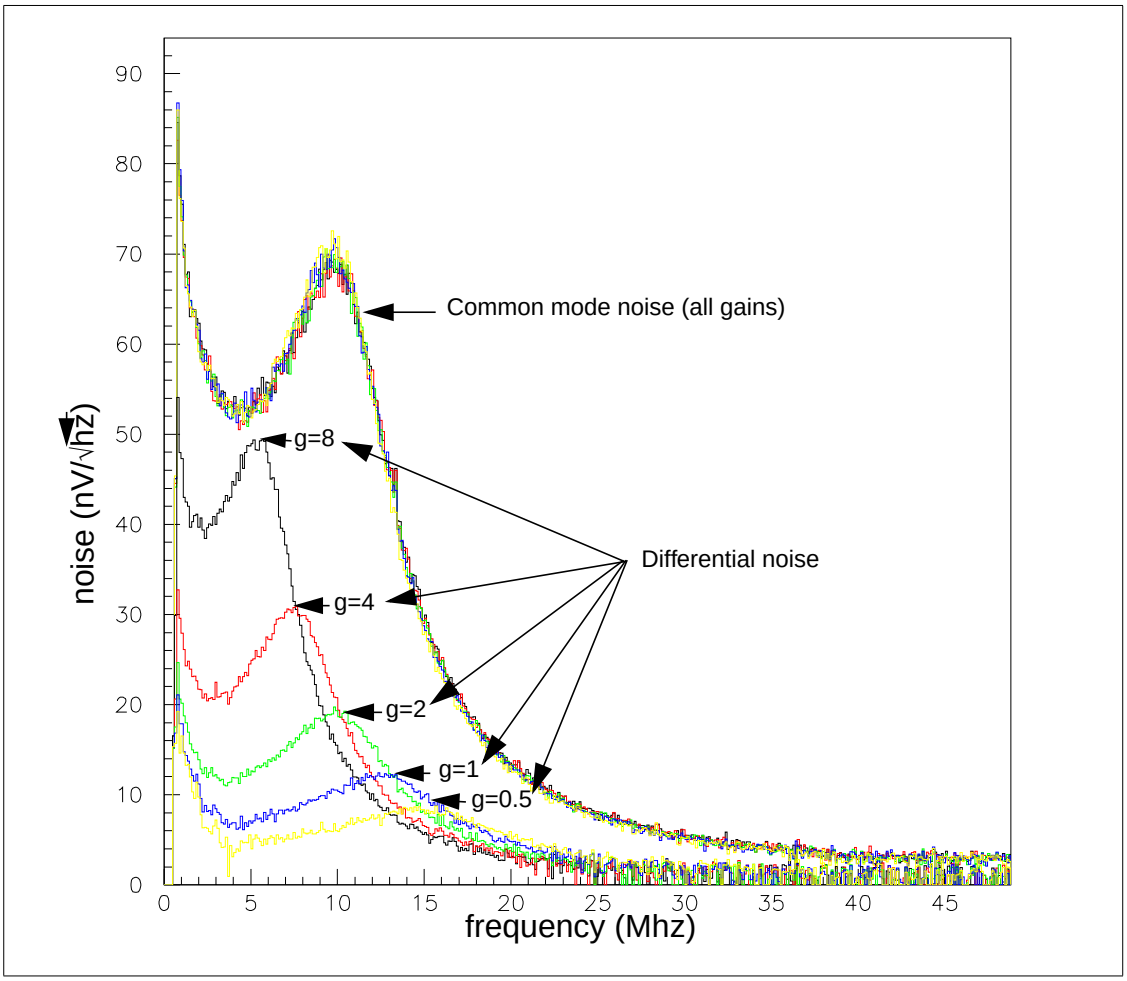

Figure 6: Output noise spectra (common mode & differential) of PGA for various gains. (Differential gain g=8 means that each amplifier of the differential pair has a gain 4).

The striking result is that the common mode noise is an “output noise” (independent of the gain), contrary to the differential noise which is an “input noise”. It is also clear than for higher gains (g>10) the differential would dominate.

3.2 baseline shifts

3.2.1 shifts induced by reset/ $\overline{\text{reset}}$

It was pointed out in the previous CDS reports [1]&[2] that the baseline of PGA or INT output was not constant and that its slope was opposite during reset and $\overline{\text{reset}}$. It was shown that given a long time in the same reset state PGA output baselines reach asymptotic values differing by 150 mV. This effect is 90% common mode and 10% differential (contrary to intuition based on the fact that the common mode is in principle fixed by feed-back, while differential mode is floating). It has been shown that INT reset has the same effect as PGA reset, although it is not connected to PGA. An explanation could be that a reset action has an effect on the reference voltage because it draw current from this voltage and that the effect on the reference voltage is seen on the PGA output through the common mode feed-back (of course the effect of PGA and INT[4] reset at the same time should be different).

3.2.2 shifts induced by the gate signal

The sequence of operations described here would be totally redundant in a system where baselines are well defined:

1. applying the reset signal forces PGA_{out}^{+} and PGA_{out}^{-} to be equal to Vref.
2. applying the gate signal during reset as in Figure 7 b) connect PGA_{out}^{+} and PGA_{out}^{-} to Vref by another path
3. after reset ($\overline{reset}$) PGA_{out}^{+} and PGA_{out}^{-} float at the same V_{ref} value (absence of PGA input signal)
4. applying the gate signal after reset as in Figure 7 a) reconnect PGA_{out}^{+} and PGA_{out}^{-} to V_{ref}

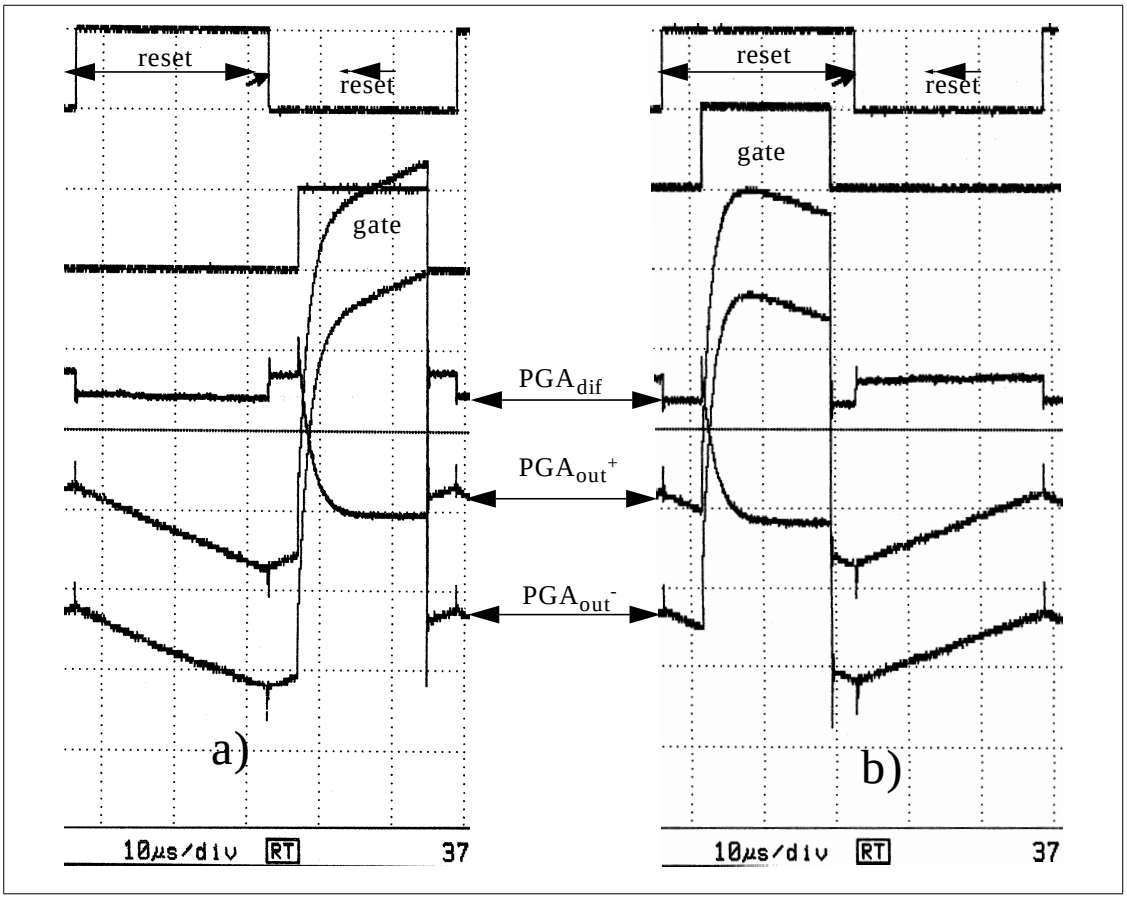

Figure 7: effect of gate signal on PGA output baseline: a) gate after reset; b) gate during reset

Instead of keeping PGA output at reset (or $\overline{reset}$) value, the gate create a 40 mV jump and worse the settling time is very long (around 5 µs). The effect is seen both in differential and common mode.

3.2.3 shifts induced by the pol signal

A similar experiment is described in Figure 8. The pol signal exchange PGA_{out}^{+} and PGA_{out}^{-}. When the state of Pol is changed during reset, PGA_{out}^{+} and PGA_{out}^{-} being both

[4] at the INT out, the PGA baseline slope introduces a quadratic term

forced to V_{ref}, nothing should happen. Similarly, when no input signal is applied to PGA, after reset PGA_{out}^{+} and PGA_{out}^{-} floating freely at Vref, nothing should happen.

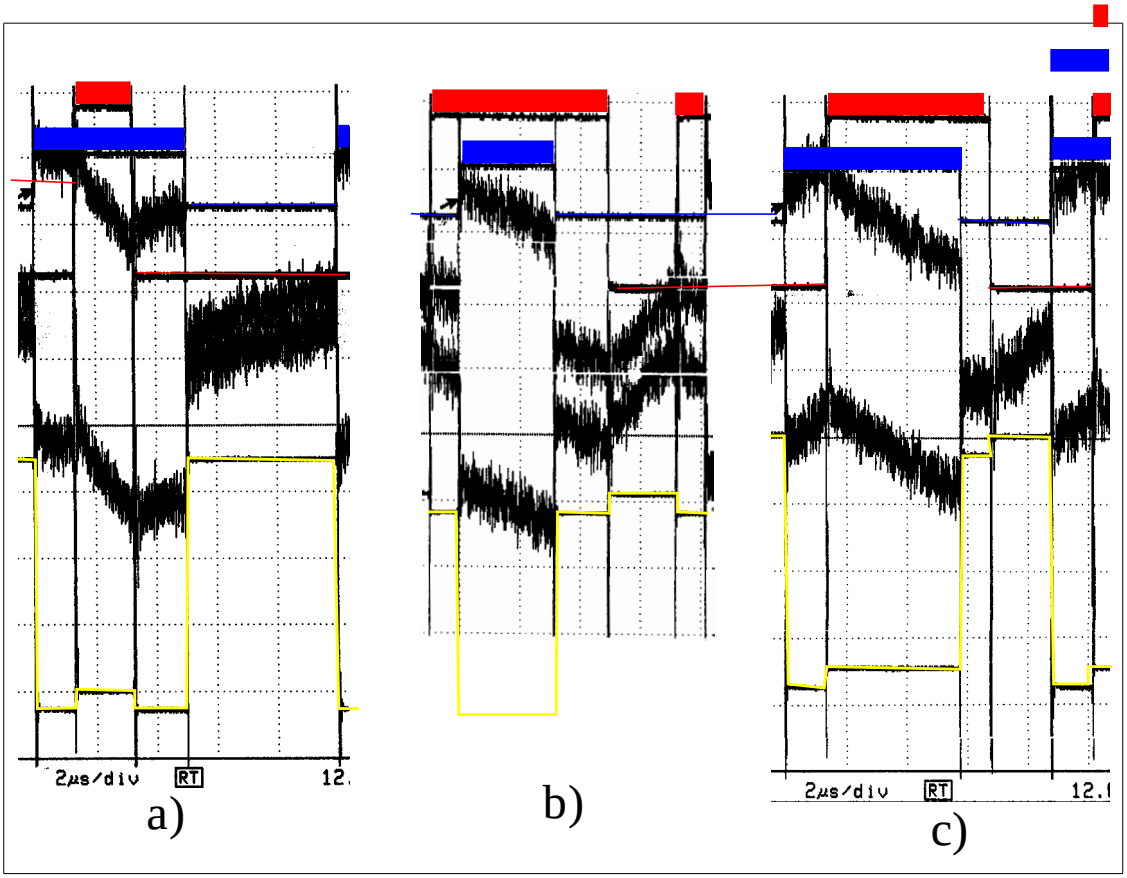

Figure 8: The change of Pol signal state (blue bar edges) provoke a jump of PGAout+ and PGAout-. a) both Pol-state transition happen during reset; b) both happen during reset (red bar); c) one during reset (red bar) and one after. The differential PGA signal is overlined in yellow.

Figure 8 shows that the baselines of PGA_{out}^{+} and PGA_{out}^{-} jump at each change of Pol signal state and that this effect is a differential mode effect.

4 Transients

We should just keep in mind that transient similar to those described in Section 2.3 are associated also to Gate and Pol signals and that at the present level (up to hundred mV and to 0.5 µs) they could spoil a CCD measurement.

5 References

1 New tests of prototype CDS chip
http://www-lpnhep.in2p3.fr/~barrelet/cds_test_02.pdf

2 Prototype CDS chip: more tests
http://www-lpnhep.in2p3.fr/~barrelet/cds_test_03.pdf

3 Discussion of the SNAP CCD e-chain
http://www-lpnhep.in2p3.fr/~barrelet/ccd_adc_01.pdf