PRELIMINARY

Prototype CDS chip: more tests

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1 Introduction

The result of a first analysis reported earlier[1] has defined some conditions to have stable operation of the prototype CDS chip and, under those conditions, two sets of problems to be tackled first (problems affecting 1- the CDS amplification chain; 2- DC stability).

We report here the next step which has consisted in a understanding qualitatively these problems.

However the main result of the analysis hereafter (with an exaggeration of the effects due to saturation) is that we need to have a better model of the circuit. The concept of this circuit is easily understood as a juxtaposition of various simple electronic elements. However the resulting system is complex. We have neither a mathematical model nor a simulation tool dealing with the stability and noise properties of this system.

2 Problems affecting the CDS amplification chain

2.1 First diagnostic

Let us recall the two kind of problems observed, which appear now as intimately related:

2.1.1 amplifier transients

For a square signal input, some transients have been observed on both amplifier outputs. They are not symmetrical when changing the amplifier input or the polarity of the signal, as seen in Figure 1.

2.1.2 stability of the amplifier/integrator assembly

When the output of the amplifier is connected to the input of the integrator the system the system becomes unstable. This instability is cured by 330 pF capacitors connecting to ground both sides of the amplifier output as well as both inputs of the integrator amplifier. This trick works only for the amplifier gain equal to 0.5 and not in a stable way.

2.2 Experimental study of the amplifier

The fine tuning of the levels of square pulses applied to both inputs of the amplifier allowed to find a variety of shapes not represented in Figure 1 and even unstable conditions as in Figure 2.

The common feature of all these shapes is a sequence of ramps corresponding to a positive slew rate $\Delta V / \Delta t = C\, I_+$ or a negative one $-\Delta V / \Delta t = C\, I_-$ with respectively C= 15 pF and I_+= 33 µA and I_-= 160µA. This very characteristic behavior, with the same currents has been

[1] http://www-lpnhep.in2p3.fr/~barrelet/cds_test_02.pdf

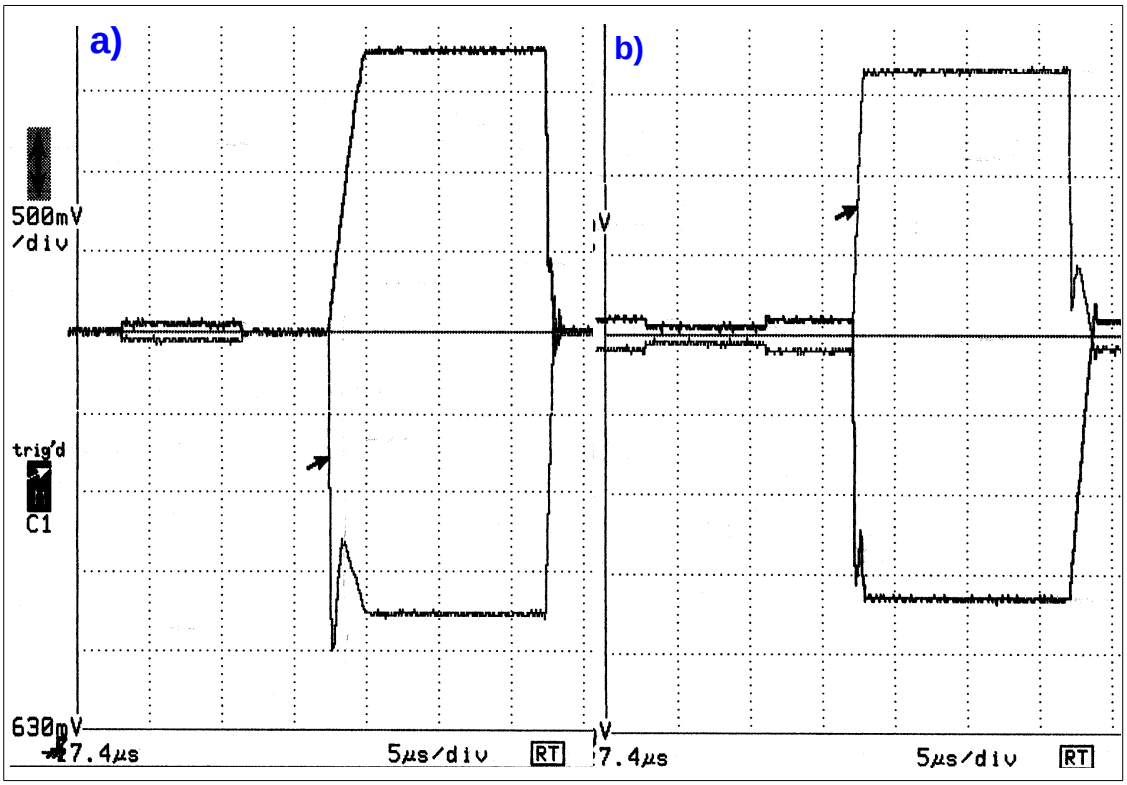

Figure 1: Both amplifier outputs are figured for a square pulse fed on either entry of the amplifier (a or b). Transient are observed on either edge.

measured with various amplitudes (100 mV to 2 V), various gains (0.5 to 8) and various polarities and balance of input signals. Moreover a trick allows to spy on the capacitive feed-back when using unipolar input, by connecting to the scope the complementary input.

The reason of this features and the value of these numbers will be found in the next section.

2.3 analysis of the behavior of the CDS amplifier

The CDS amplifier functional layout is represented in Figure 3. The corresponding electronic circuitry is shown in Figure 4.

Approximate gains are indicated on the functional layout. The analysis of the circuit as it works with “fast” fronts, i.e. with a rise faster than 0.5 V/µs, shows a complete saturation of the second stages of amplification C_p and C_n which yield the limiting currents I_+= 33 µA and I_-= 160µA observed in Section 2.2.

The behavior of Figure 2 is easily understood: the output signals, out_p and out_n, follow exactly the voltage at the input of the follower amps D_p and D_n. The voltage gain from the inputs in_p and in_n to the output of the second stage C_p and C_n is around 7000. For a step input above 200 mV these amps are immediately saturated. Then the loading of the 15 pF capacitors by the limiting currents I_+ and I_- produces the asymmetric ramps observed. The capacitive feed-back transforms these asymmetric voltages into asymmetric feed-back charges on the input capacitors.

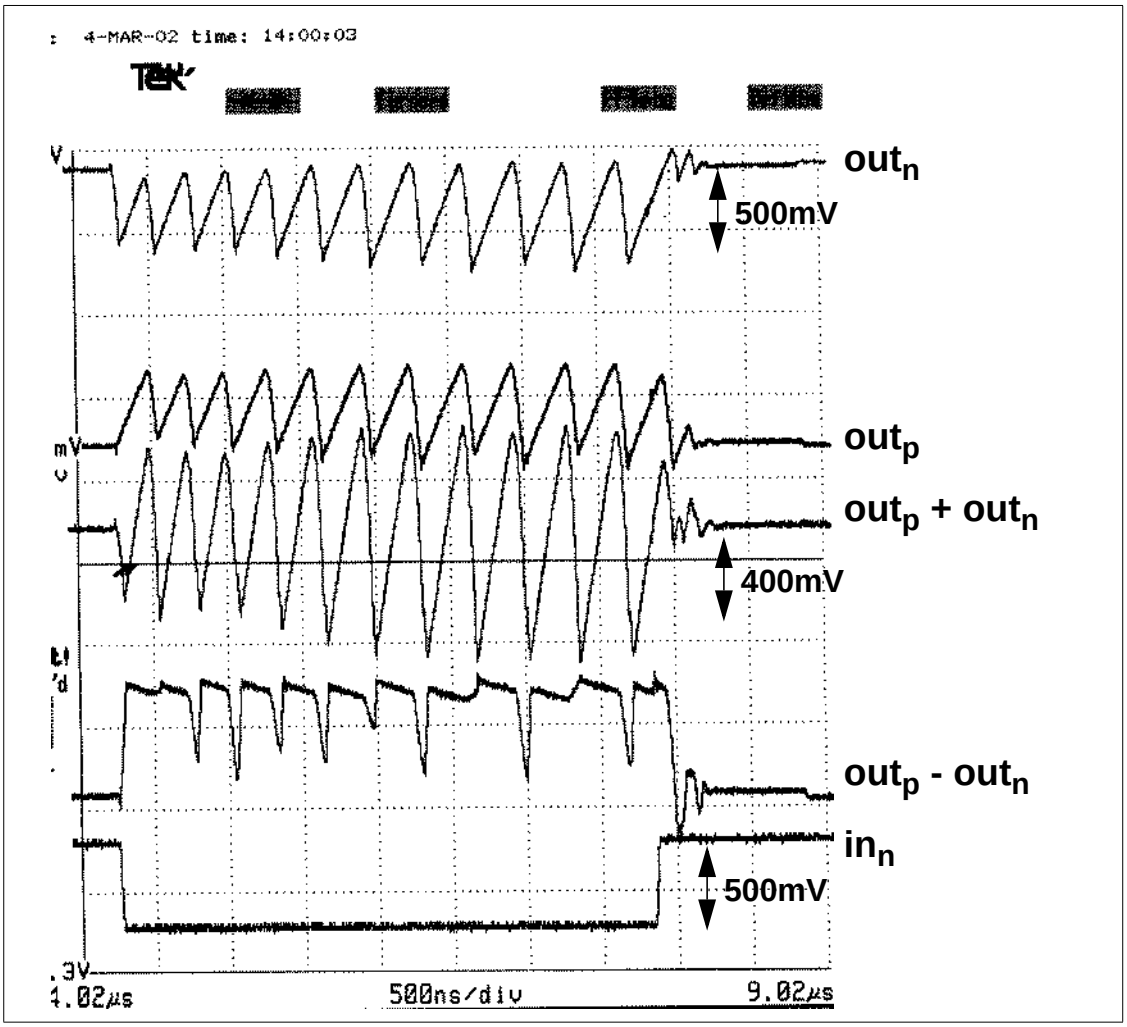

Figure 2: Response of the CDS amplifier to a bipolar square pulse (in_p=-in_n) for an amplitude corresponding to an unstable behavior. The two outputs (out_p and out_n) are shown, as well as their sum and difference.(with a slightly different scale)

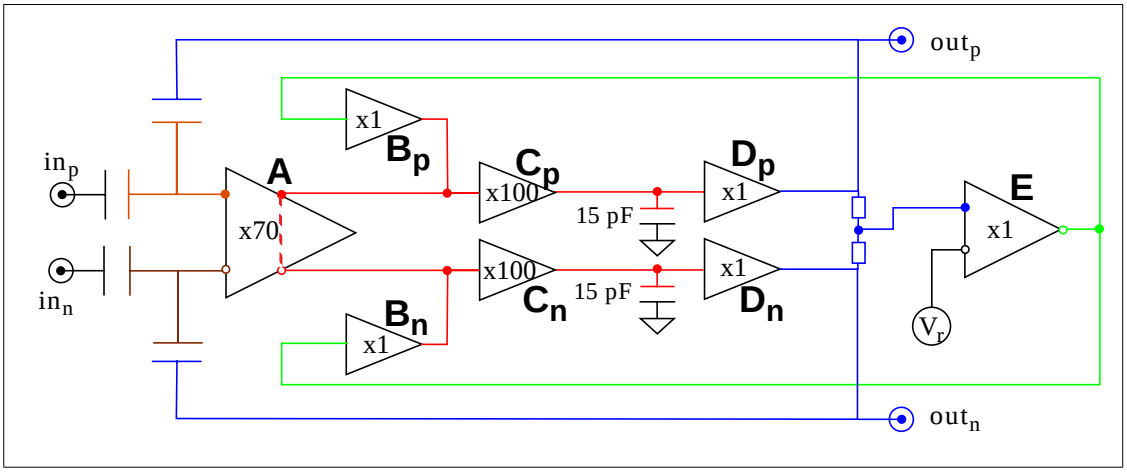

Figure 3: CDS amplifier: functional layout. The parts of the circuit which are DC coupled appear in the same color.

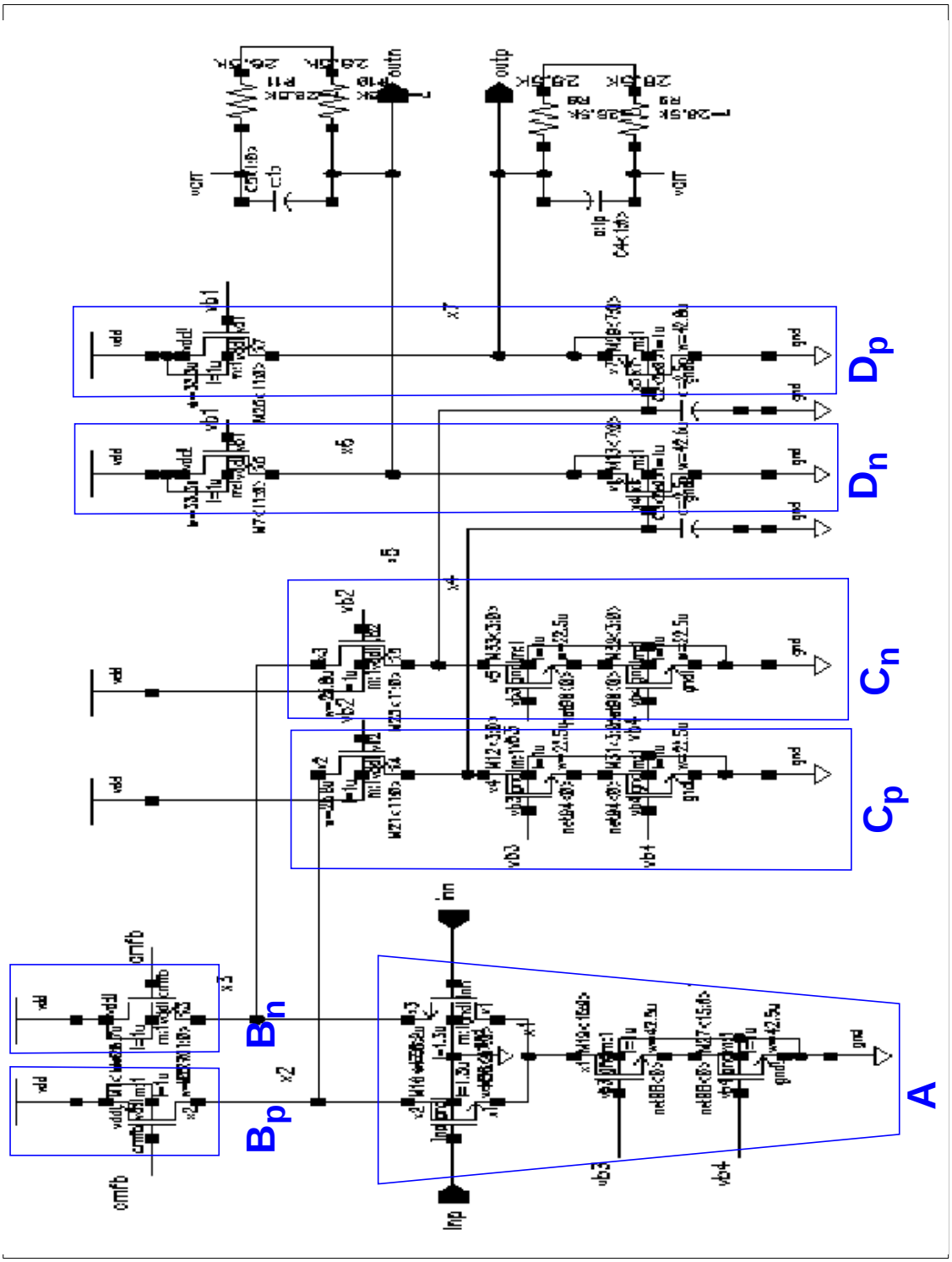

Figure 4: CDS amplifier electronic layout. Each labeled box contains the components needed to perform the function defined by the same label in Figure 3

3 DC stability

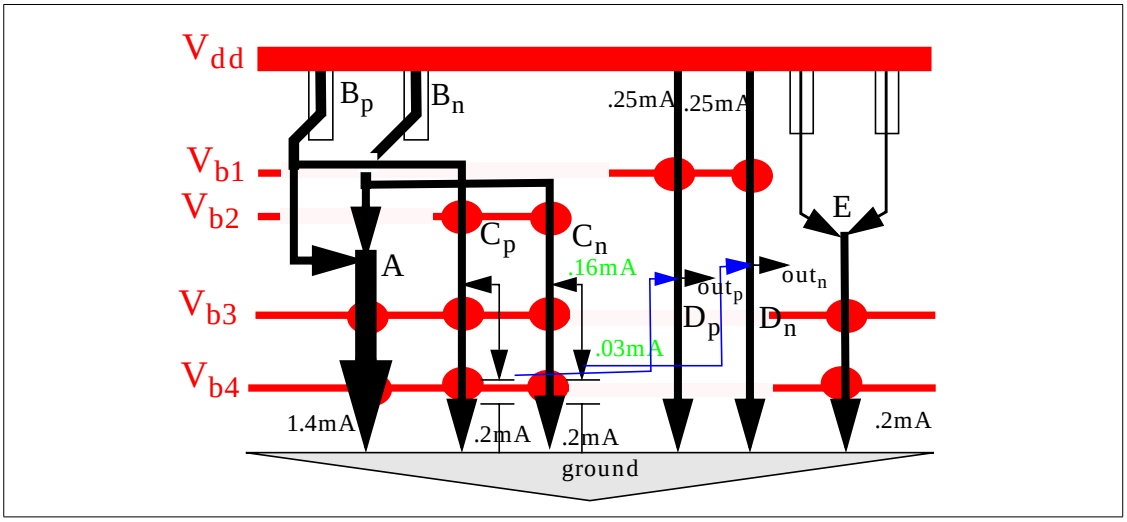

Figure 5: Typical currents and voltages in the CDS amplifier (in green: limiting transient currents)

3.1 First diagnostic: baseline modulation problem

This effect is the cause of the polynomial subtraction developed in our previous noise analysis. The 20 µs time constant is transformed into 200 µs by decoupling the V_{ref} potential. Its maximum amplitude is about 110 mV as seen inFigure 6.

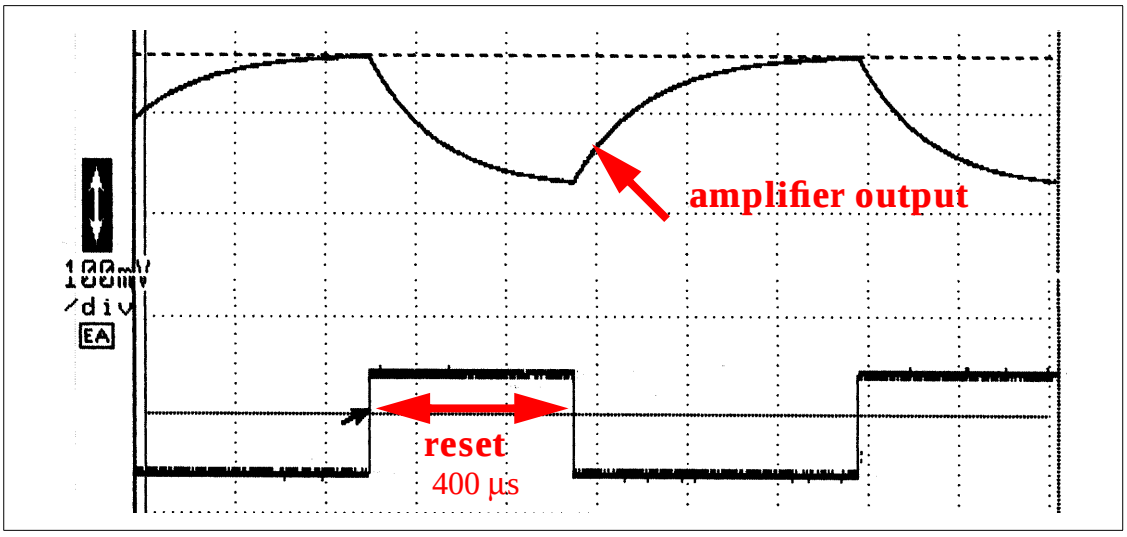

Figure 6: Baseline modulation by the reset in absence of input signal

This baseline modulation is mainly a common mode effect. It appears also in the differential mode divided by a factor 10. When we apply a square signal of small amplitude on the input it appears on both outputs added (or subtracted depending on the polarity) but not in a perfectly symmetrical way. This means that the common mode output signal is no more perfectly square.

3.2 analysis of the DC behavior

The relation between DC levels of various segments which are not DC coupled (in different colors in Figure 7) is established during the reset phase. This is acomplished when closing

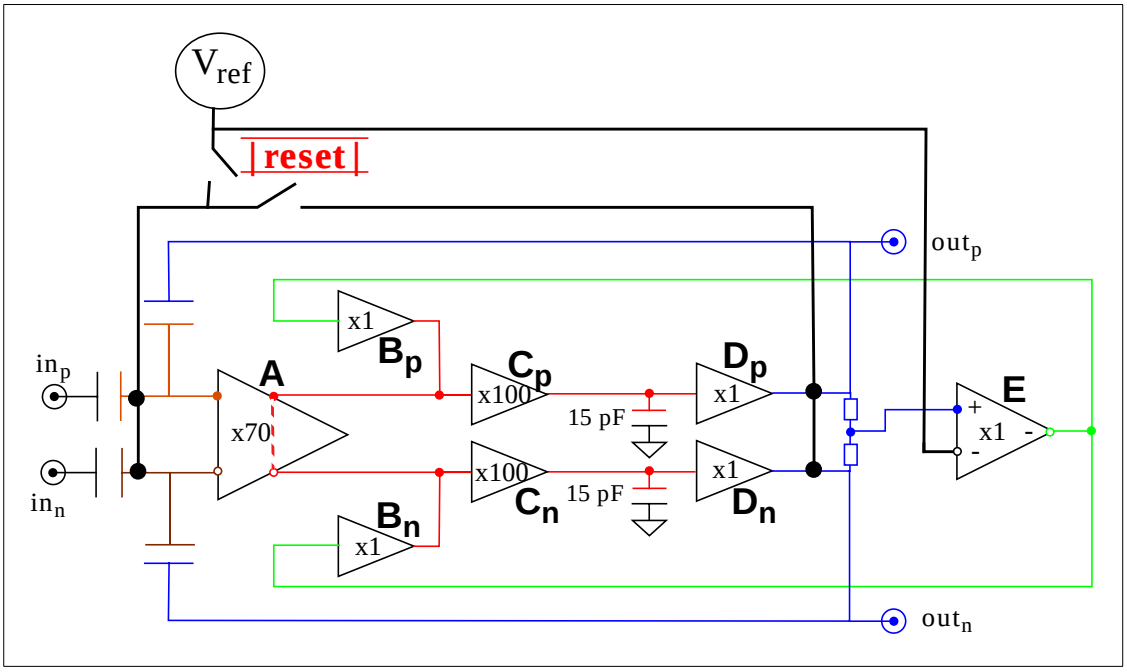

Figure 7: CDS reset mechanism:

the reset switch which is supposed:

1. to bring to the V_{ref} voltage on both out_p and out_n. The average of these two outputs is connected to one input of the differential amplifier E. The other input of E being also equal to V_{ref} ,the output level of E is then defining the “common mode =0” condition which characterize the neutral state of the common mode feed-back. This is “common mode =0” level is reinjected on both input amplifiers (in fact it controls the gates of B transistors which are loading both amplifiers A and C).
2. to bring also the V_{ref} voltage on both inputs of the CDS amplifier, which means that the feed-back capacitors have a null charge and that the amplifier stages up to the input of the follower amplifiers D_p and D_n are in a reference state, with a reference charge on the 15pF capacitors.

Here comes the inconsistency: The two power amplifiers D are competing with the voltage generator V_{ref} to fix the output level. There is not a catastrophy because by simulation of the circuit J.F.G. has computed components yielding the V_{ref} as the reference output of both amplifiers D, therefore the difference between competing voltages is just the difference between simulation and reality. The common mode voltage resulting from a compromise between competing voltages (one has still to compute the dividing bridge) is stored on the V_{ref} decoupling capacitor. This explains the time constants seen on Figure 6.
