Status of CDS DMILL Prototype

History and Goals of the Project:

- CDS prototype was designed by Carl Grace in 1999
- translated into DMILL 0.8 m by J.F. Genat, with LBL support in 2000
- delivered in june 2001 and tested by J.F.Genat and R.Sefri

- proof of feasability of the integration of a full CCD analog readout
- measurement of some figures of merit of the DMILL radhard process
- check of the integration of the classical CDS circuitry

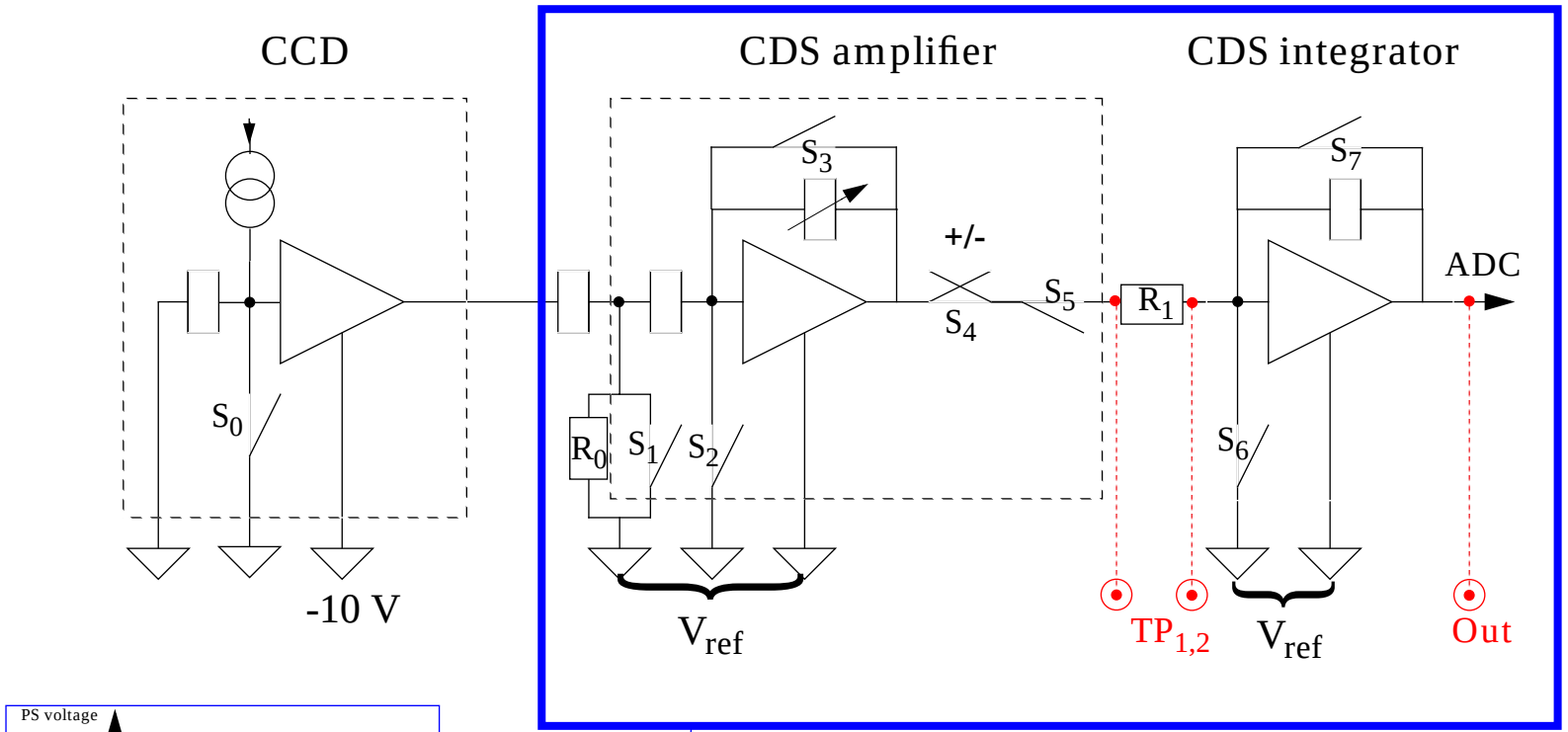
Scope of this Presentation:

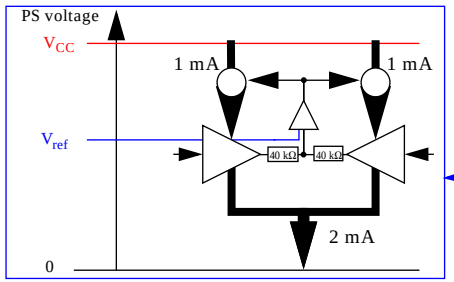
- results of january 2002 tests[(1)] and triggering of new orientations

[(1)](J.F.Genat, R.Sefri, A.Secroun et E.B.)

text found at http://www-lpnhep.in2p3.fr/~barrelet/cds_test.pdf

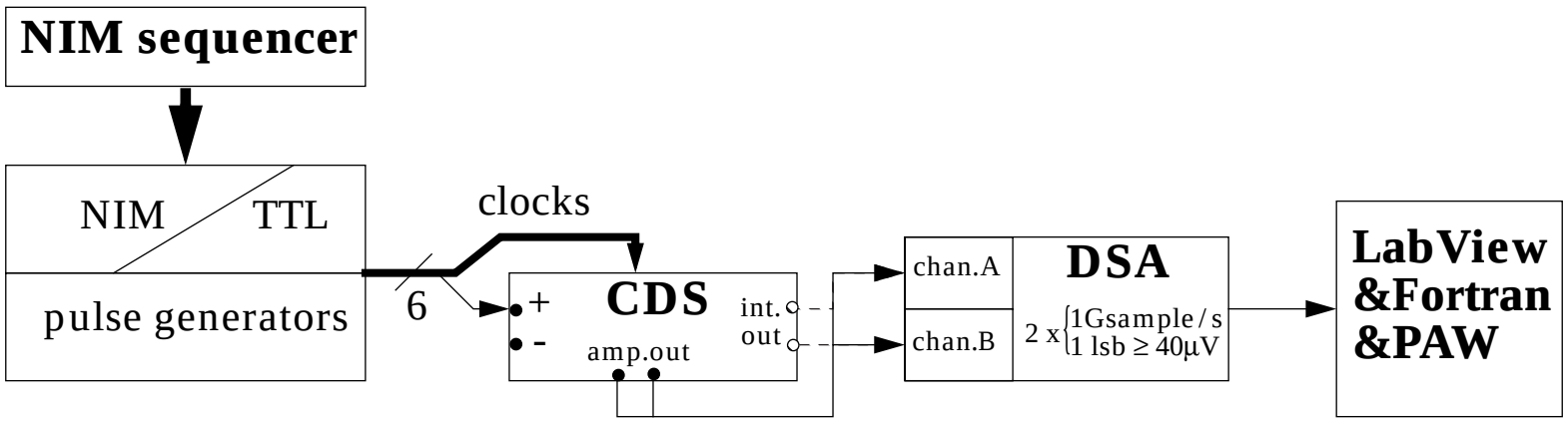
CDS IN THE CCD READOUT CHAIN:



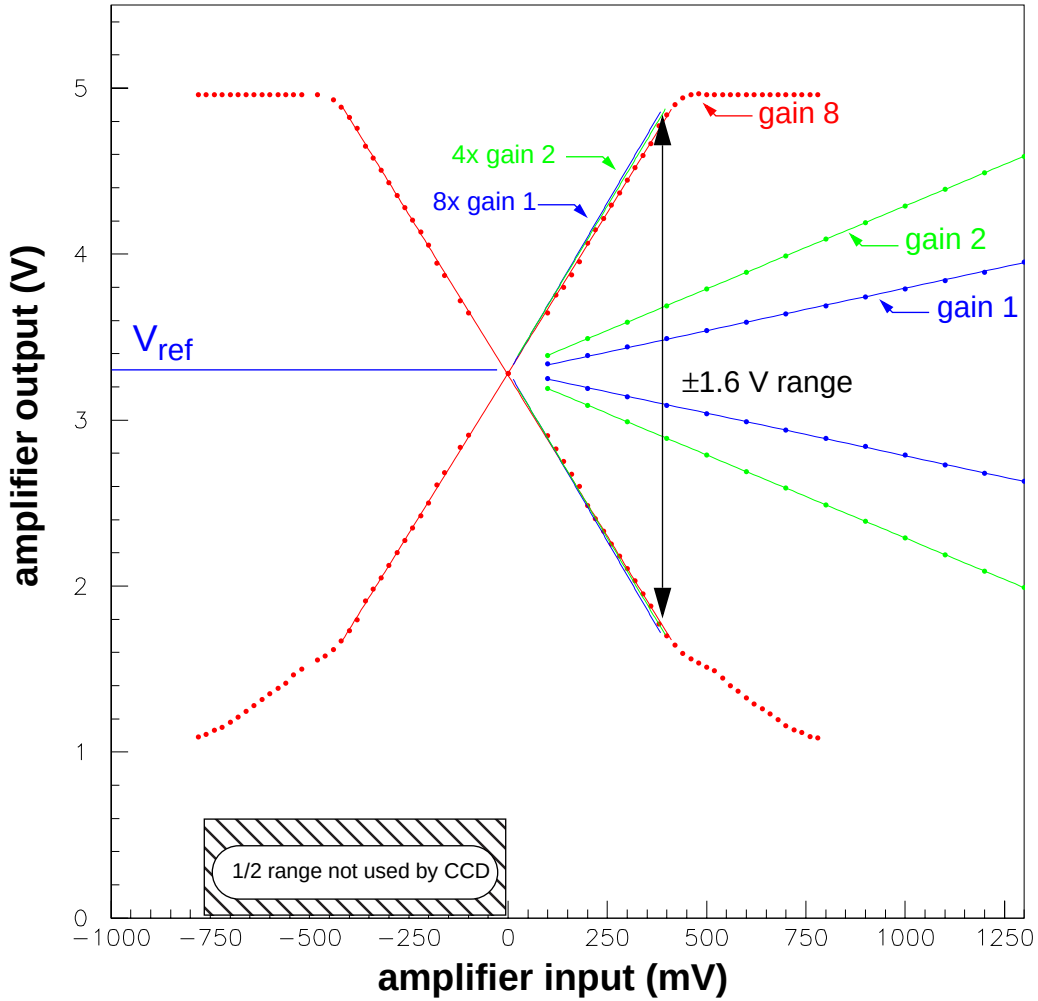


One half of CDS

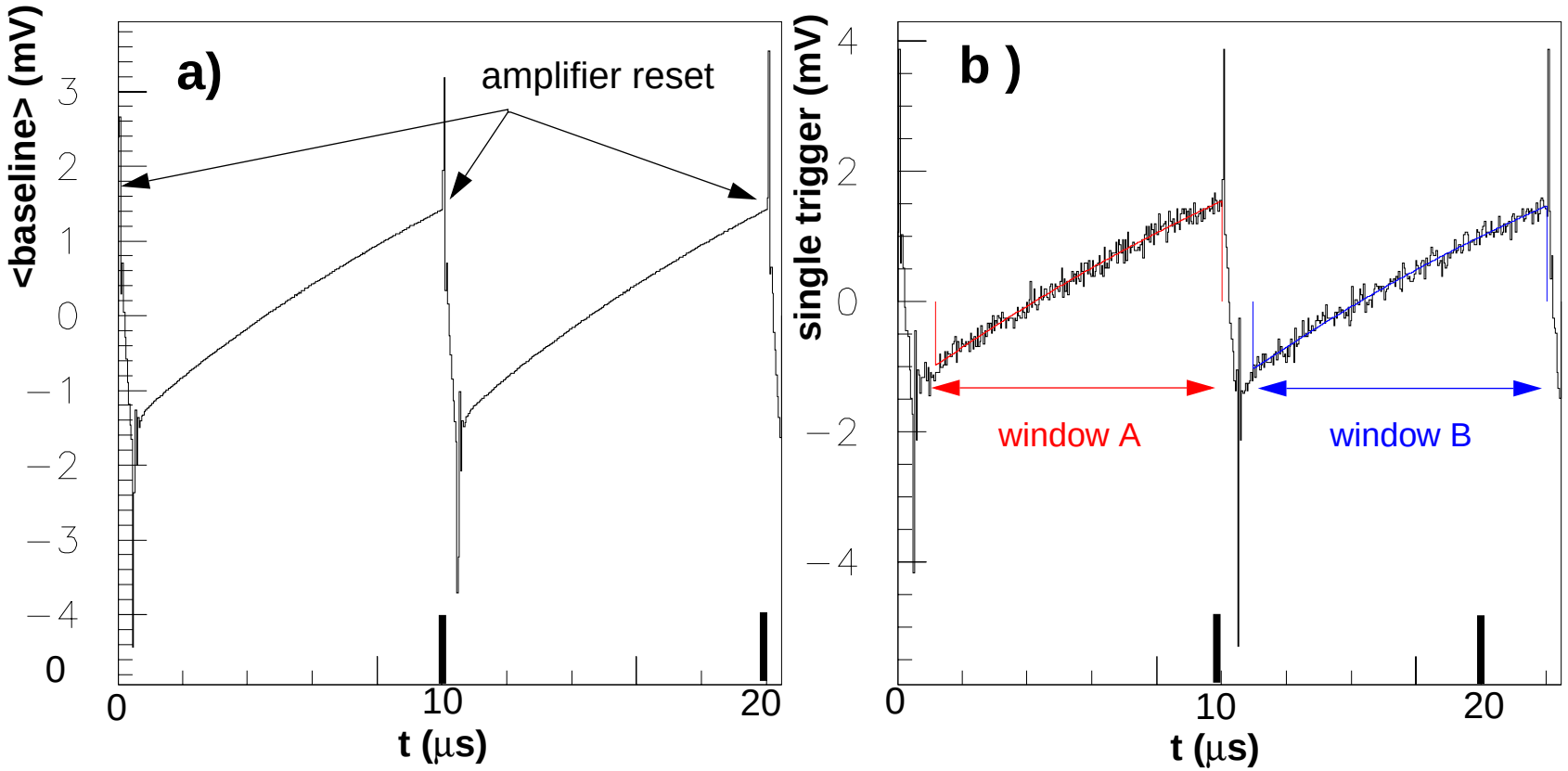
NEW TEST SETUP (JANUARY 2002)



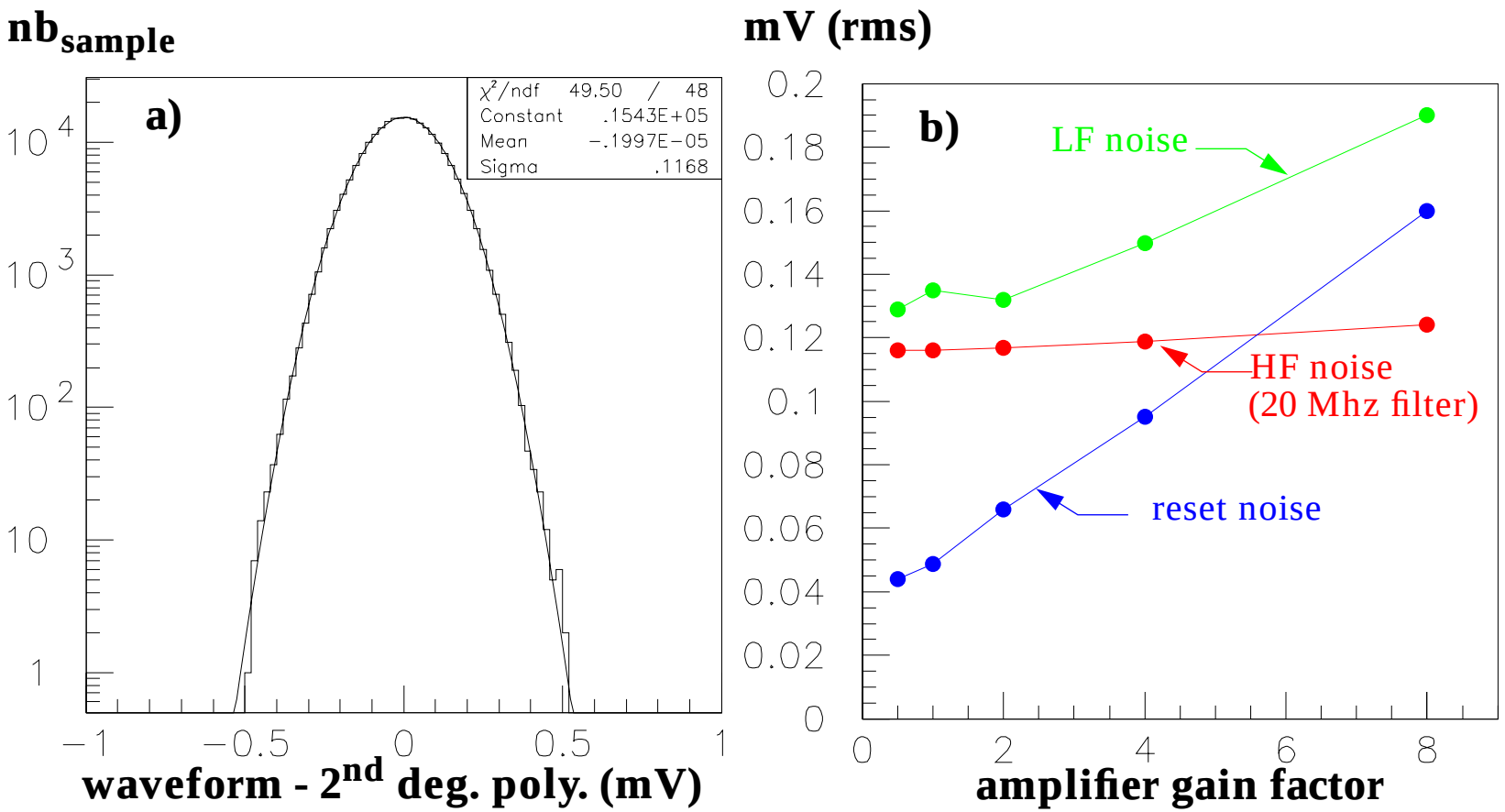
LINEARITY ~~ GAIN ~~ RANGE (AMPLIFIER)



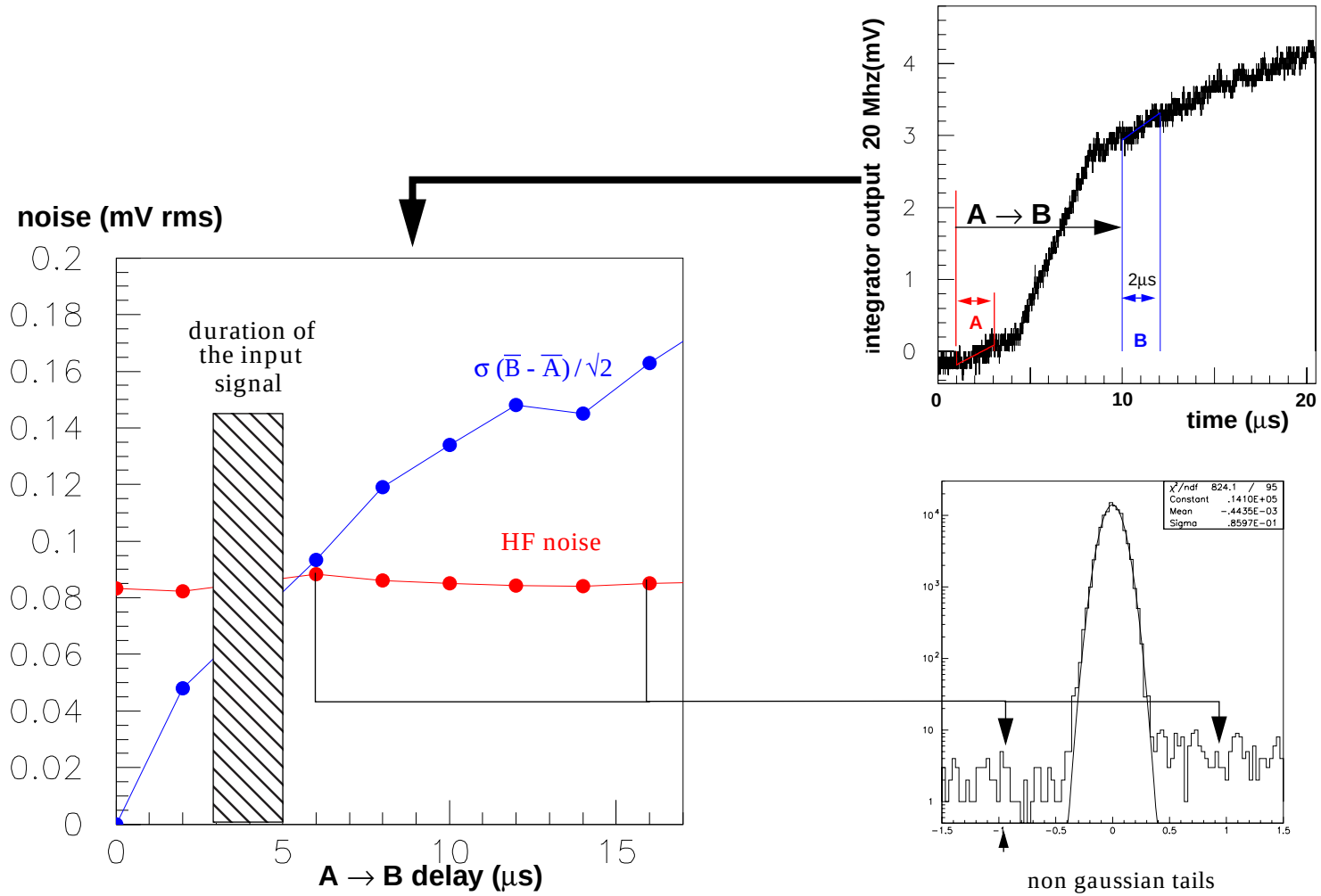
AMPLIFIER NOISE 1



AMPLIFIER NOISE 2

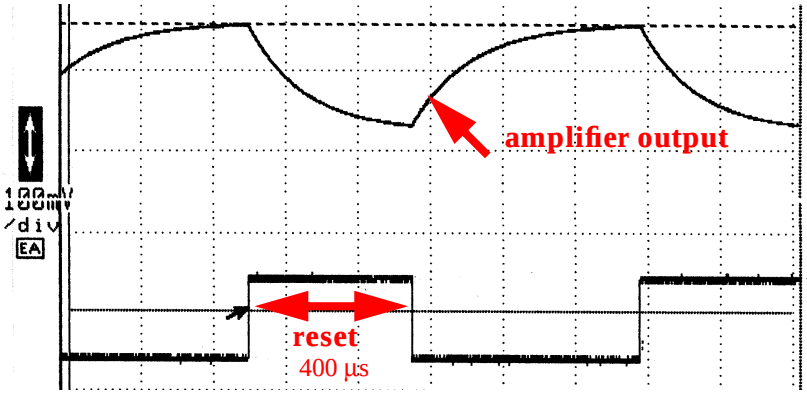


INTEGRATOR NOISE

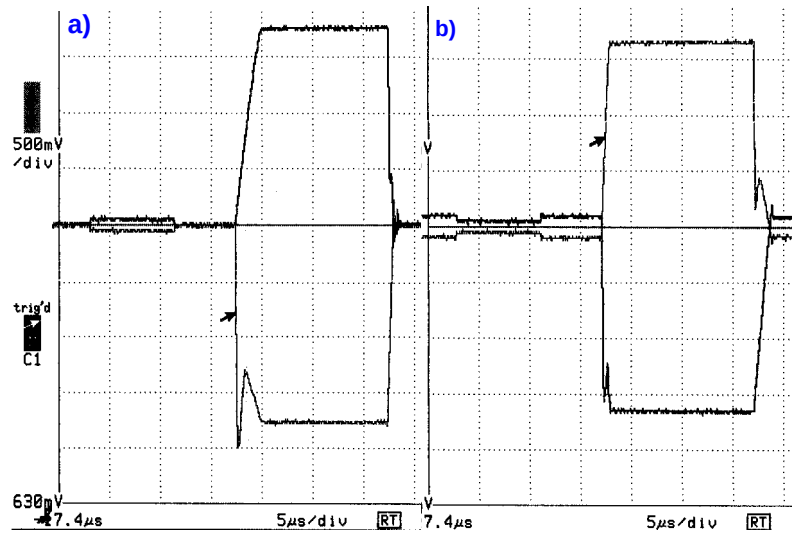


PROBLEMS

- **Baseline modulation by reset** →



- **transients on edges (amplifier out)** →



- **unstability of cds assembly (amp+int)**

- **etc...**

NOT YET REPRODUCED BY ELECTRONIC SIMULATION

PLANS

Analytic approach:

- simulate the problems previously mentioned
- study of transients and timing constraints due to each switch, one at a time
- time constraints coming from the interaction between two clocks

System approach:

- optimization of the time diagram
- optimization of the gain chain
- completion of our chain (CCD -CDS -digitizer)
- comparison with other (simpler?) analog chains

CONCLUSION

(please take first the positive aspect of each following statement)

- Electronic noise seems a factor x2 above simulation (itself a factor x2 above CCD output). If this hypothesis is verified, it leads to a waste of ADC range *(all what can reasonably be predicted works well)*
- Our CDS prototype is at the top of the complexity scale. It might be difficult to understand all the problems only by signal analysis joined to electronic simulation *(they did pretty well with this complex circuit on the first try)*
- It is necessary to integrate all these elements in order to design a realistic analog chain for SNAP. In particular multiple gains would have a profound impact on this chain. A global perspective is important for us to focus our tests on real issues *(easier to simplify rather than the contrary)*