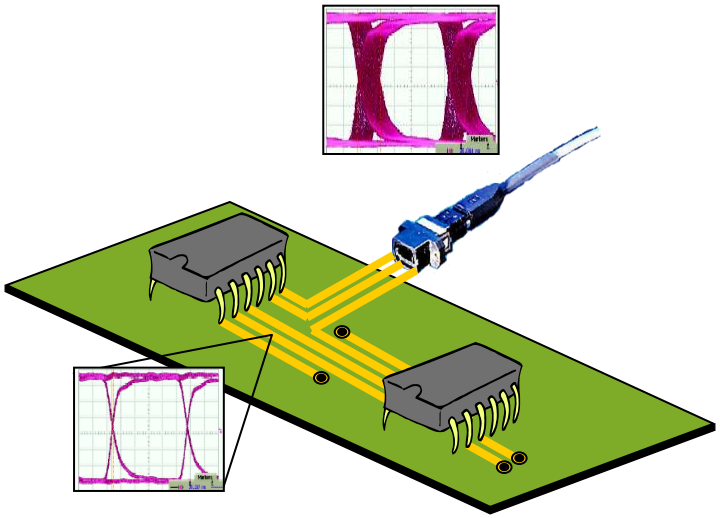
Agilent Signal Integrity Seminar 2010



High Speed Serial Links from Debug to Compliance
Eye diagram and Jitter Analysis

Presented by:
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Digital Design Application Engineer

Agilent Technologies

Goals

In the new world of high-speed serial interconnects

- **Meet objectives for cost, performance and reliability**
- **Finish your project on time and in budget**
- **Ensure Product Interoperability with other equipments**

Agenda

Why Mesure Jitter

Jitter Concept

Bus Topologies

Quick Serial Link Debug Overview:

Eye Diagram

Mask Test

Isolating MAsk Violations with 8B/10B Decode and Jitter Trend

Digging Into the Jitter Understanding

Jitter Analysis Level One: Jitter Trend

Why Measure Jitter?

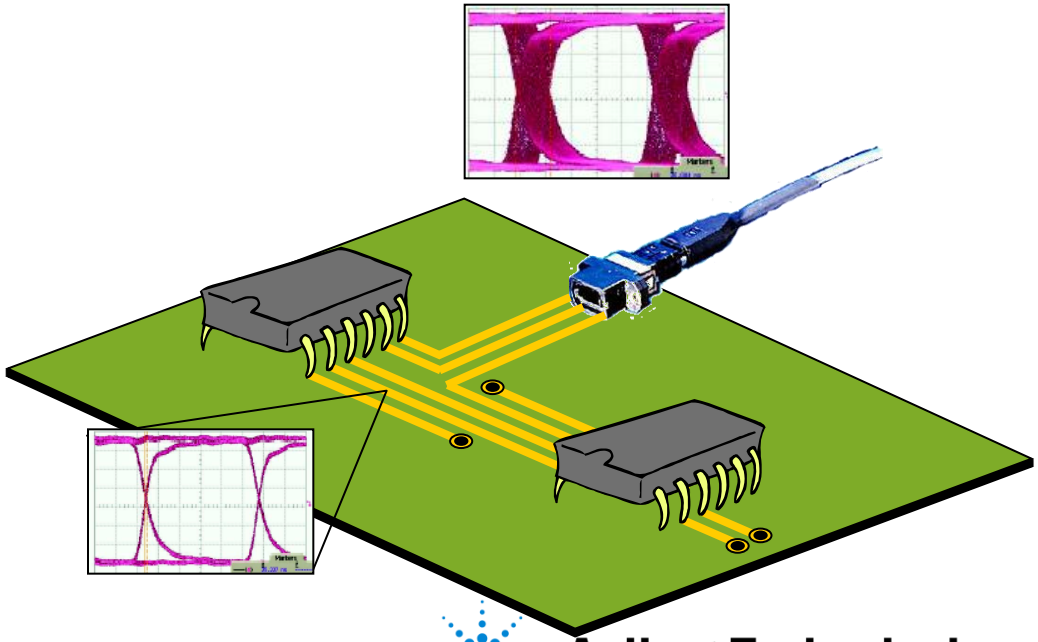
- **Determine the probability of how often a design will meet a bit error rate specification (10^{-12} BER typically desired).**
- **Understand the source of jitter in order reduce jitter to meet a timing budget requirement.**
- **Test for compliance to ensure compatibility between components from multiple vendors.**
- **Ensure that digital designs have the timing margins to operate reliably 24 hours a day.. 7 days a week.. without crashing!**

Concept of industry standards for jitter

There are up to three sides to the problem

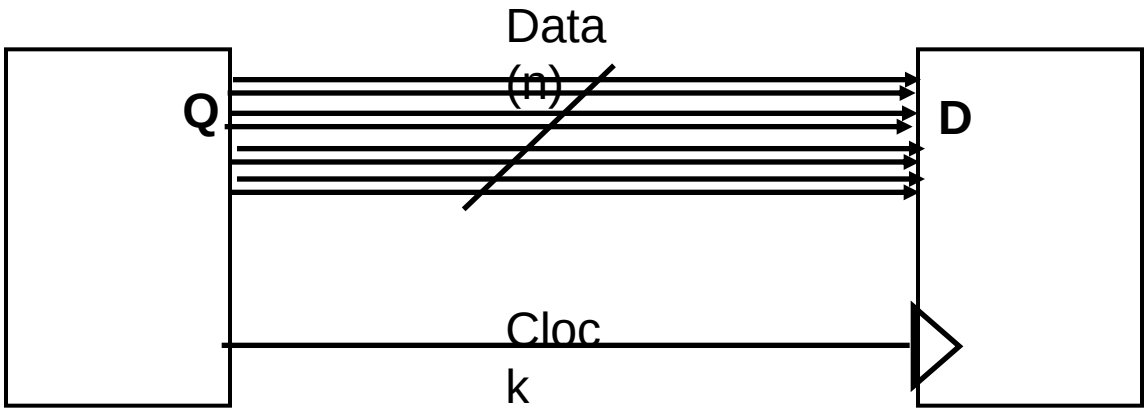
- **How much jitter should the transmit side produce**
- **How much jitter can the receive side tolerate**
- **How much degradation is acceptable from transmission line in the case of an external cable (SATA,HDMI,DISPLAYPORT,USB…)**

A well designed standard specifies each side properly to guarantee system level performance (bit-error-ratio)



But What bus Topology are facing?

Parallel Data Bus With Explicit Synchronous Clock

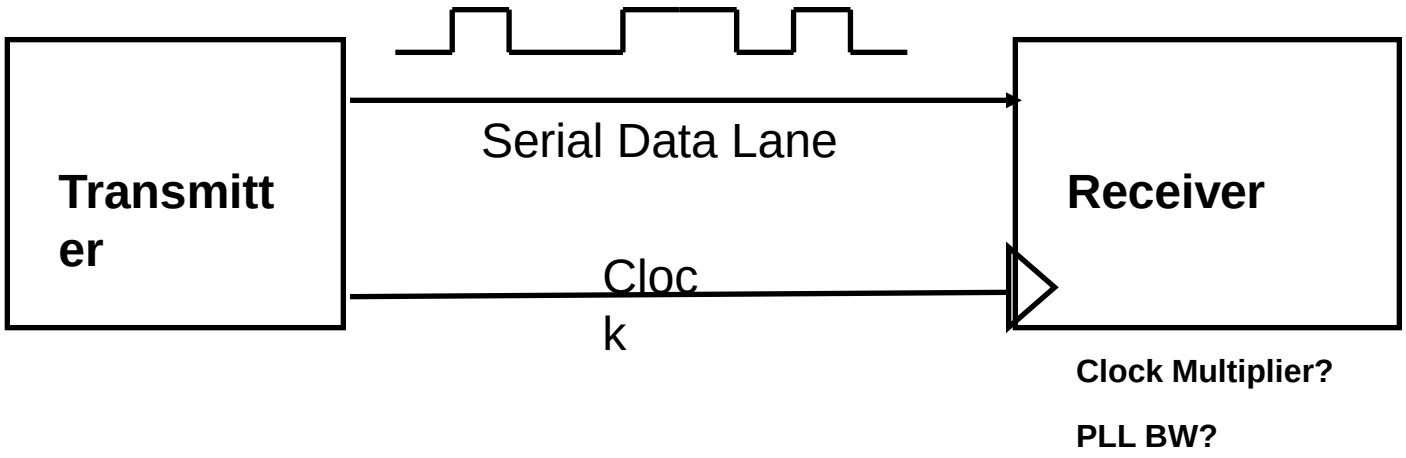


-Bus of Parallel data lines at specific Datarate

-Clock line synchronous to Data Bus

Exemples: Legacy PCI, GPIB, SDRAM,…

Serial Data With Explicit Clock

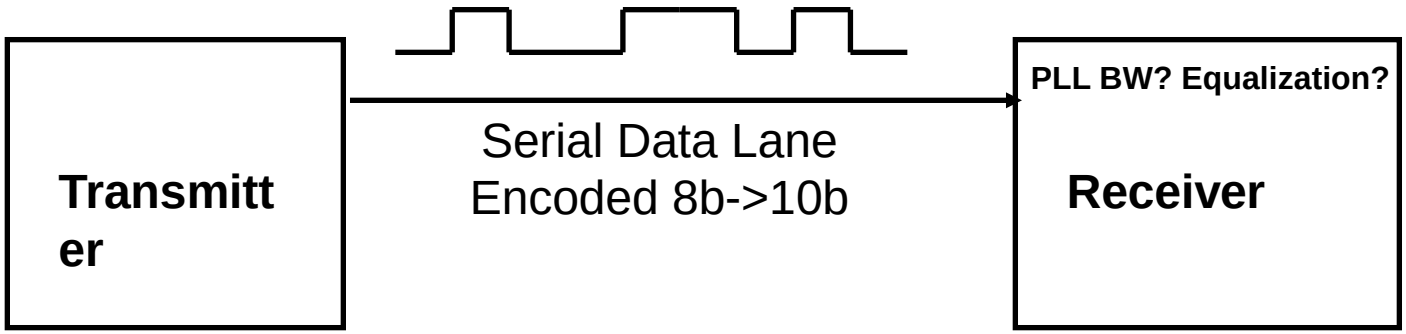


-One or several Serial data lines at specific Datarate

-Clock line can be at (Datarate)/N

Exemples: I2C, SPI, DigRF, HDMI, PCI EXPRESS 8Gb

Serial Data With Embeded Clock



-No physical Clock Lane provided to receiver

-One or several Serial data lines at specific Datarate

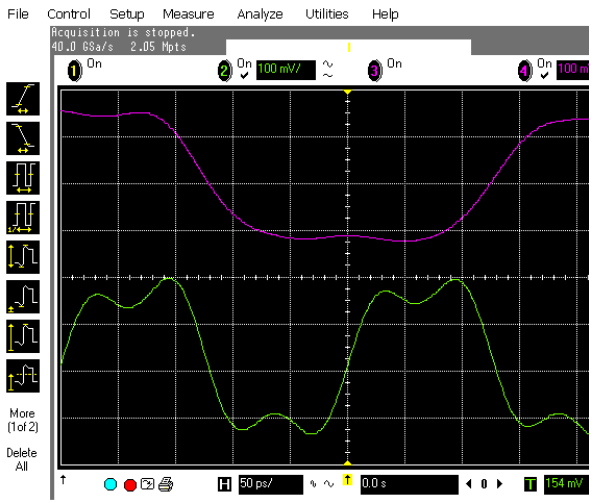
-Data encoded 8B/10B NRZ

Exemples: USB,SATAI/II,PCI-EXPRESS, DISPLAY PORT

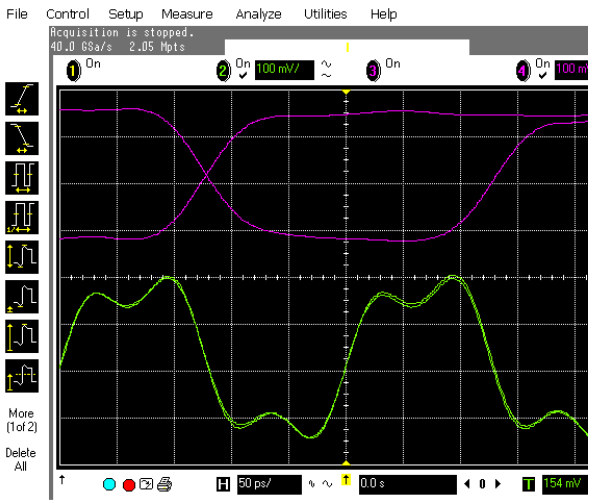
Analyzing jitter: The Famous Eye Diagram

- Start with the eye diagram
- The easiest way to get an overall idea of the quality of the serial signal
- Trigger on Clock signal (if available) as the rough first pass to build Eye Diagram
- Eye Diagram is the superposition in the middle of the screen of 3 bits
- Multiple case combined form the Eye (000,001,010,011,100,101,110,111)
- Preceedig bits might impact the ones your seeing this is called Inter Symbol Interferences
- Use Clock Recovery with PLL Emulation on 8B/10B signal and memory folding to build eye

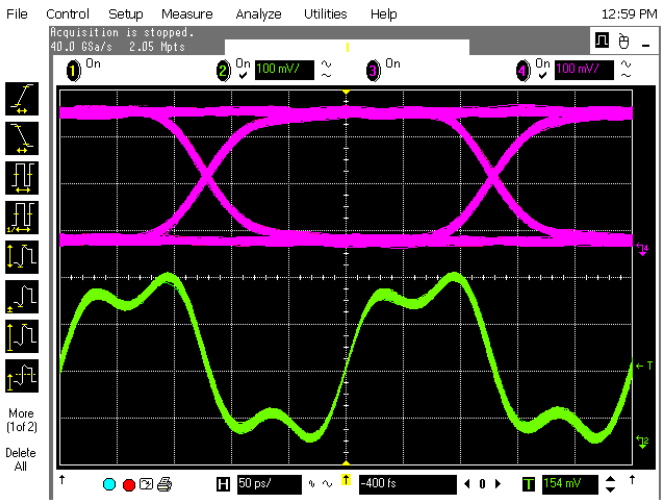
Building an Eye diagram the synchronous way: Explicit Clock used as Trigger



101 Sequence



011 Sequence



Overlay of all combinations

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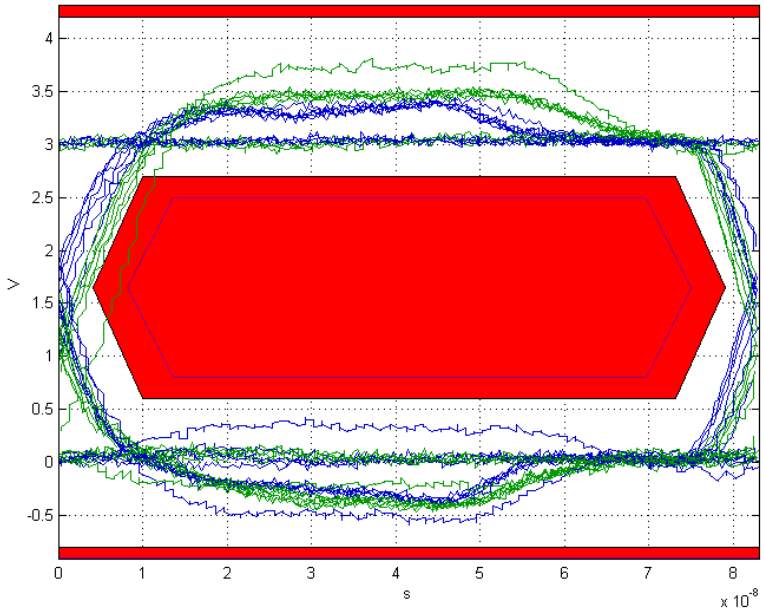
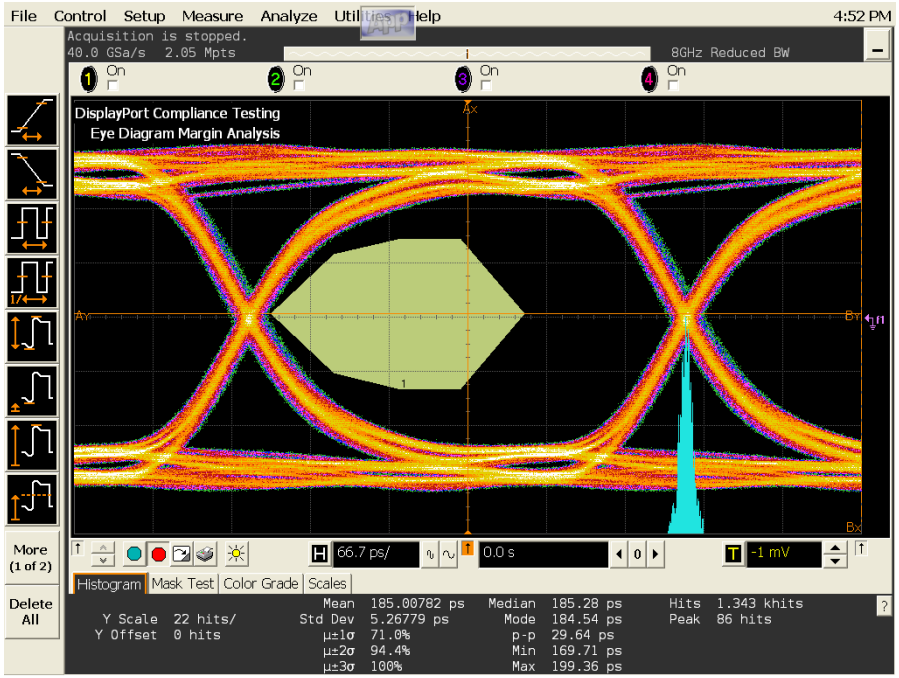
What represents “good enough”?

- The eye-mask is the common industry approach to measure the eye opening
- Failures usually occur at mask corners
  - But what is cause of failure?



Violating USB FS 12Mb/s Eye Diagram



Good Displayport Eye Diagram

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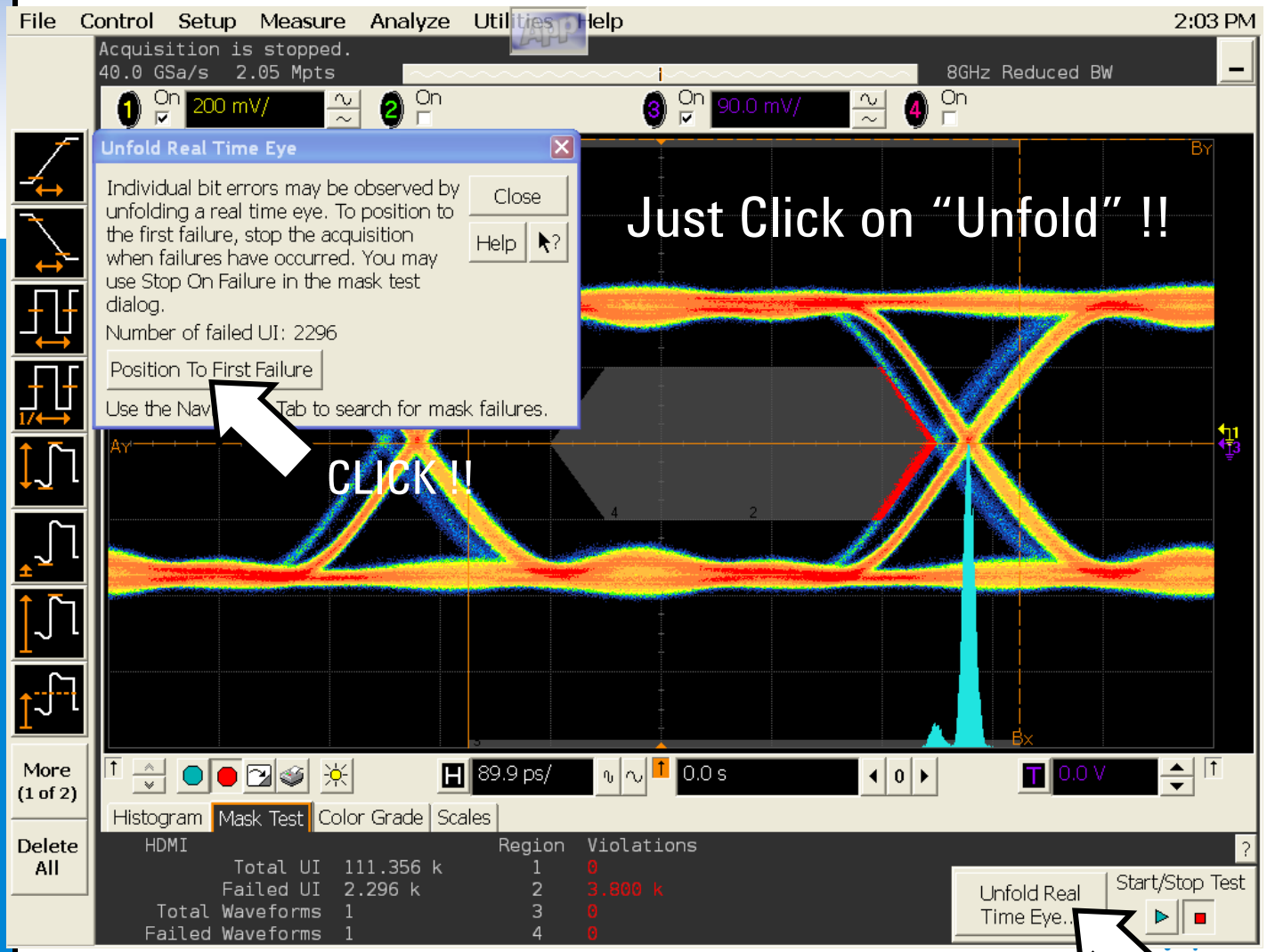
Next Gen Debugging: Let Us Begin with an Eye Pattern
What will You Want NEXT, after Finding Mask violations?



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Next Gen Debugging: By "Unfolding the Mask", Eye Pattern Failures are Correlated with Real Data and Clock Info

Not only the data mask failures are identified, but it can be correlated with the clock.

Plus, you can scroll through each failure by clicking the navigation button.

DATA

CLK

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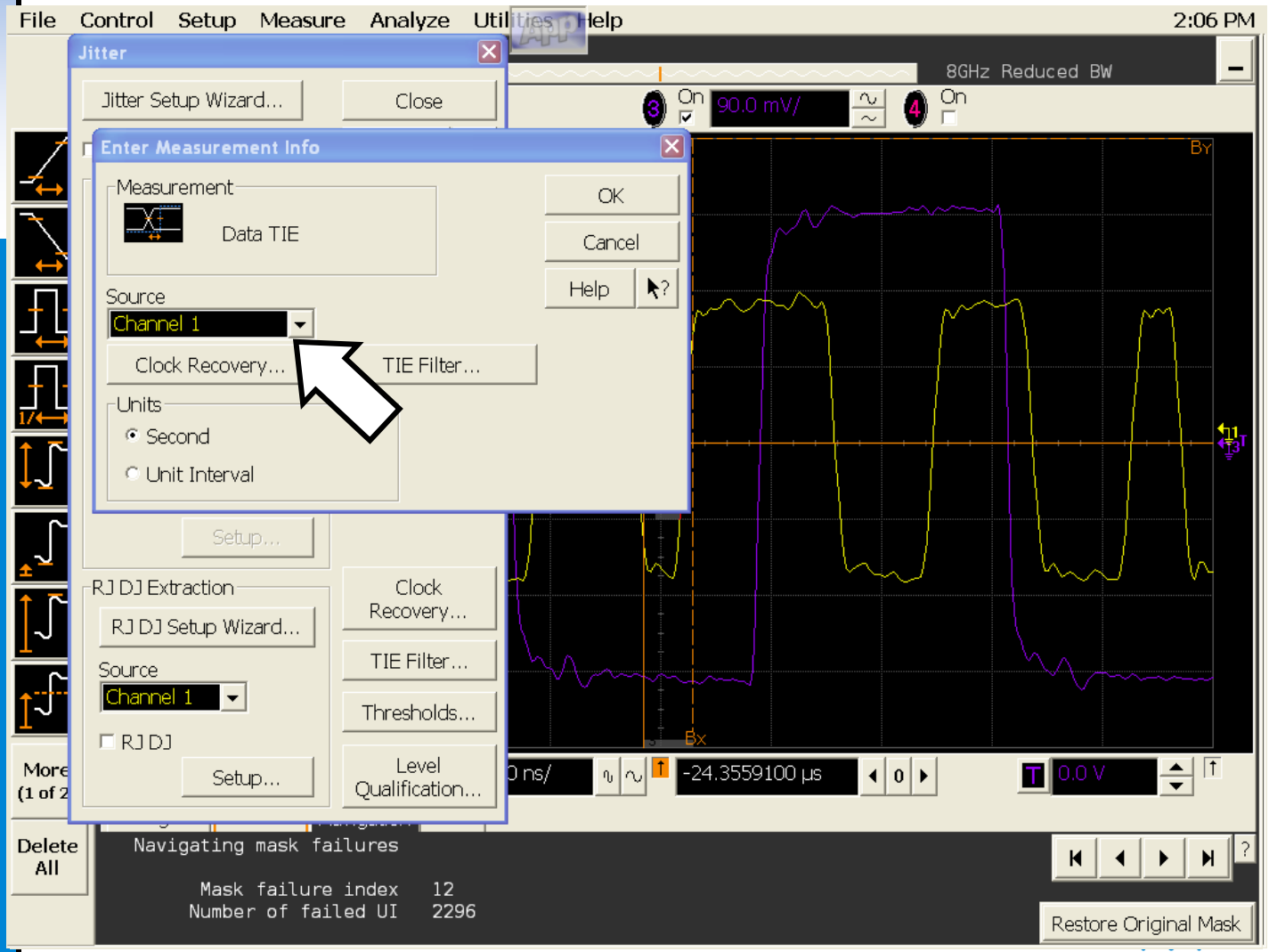
Next Gen Debugging: Infiniium Debugging Solution Supports Jitter Trend correlation with Unfolded Mask



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Next Gen Debugging: The Failure Correlations Among Data, Clock and TIE Jitter Trend, *Simultaneously!!*

DATA

TIE Jitter Trend

CLK

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Can your debugging tool reveal this much information?

Next Gen Debugging:
Debugging Continues… Found a Large Step in the Jitter Trend

TIE Jitter Trend

DATA

CLK

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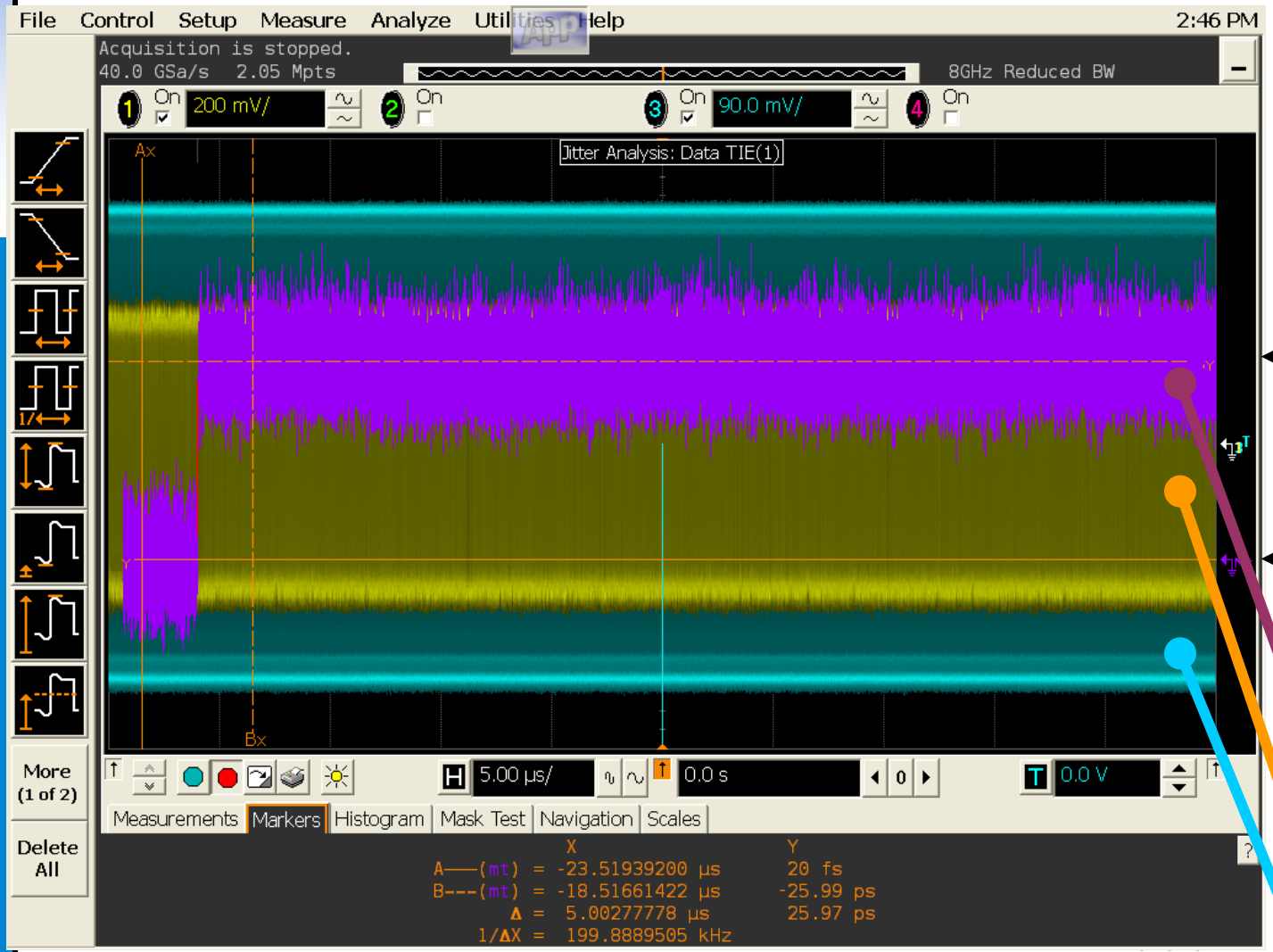
Next Gen Debugging:
Debugging Continues: The Lower Step has a Larger Jitter



TIE Jitter

20fs

-25.99ps

TIE Jitter Trend

DATA

CLK

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Next Gen Debugging:
Correlation of Mask Unfold Data vs. Jitter Size

Let's scroll through the violations of unfolded mask and correlate the violations with the jitter trend.

CLICK !

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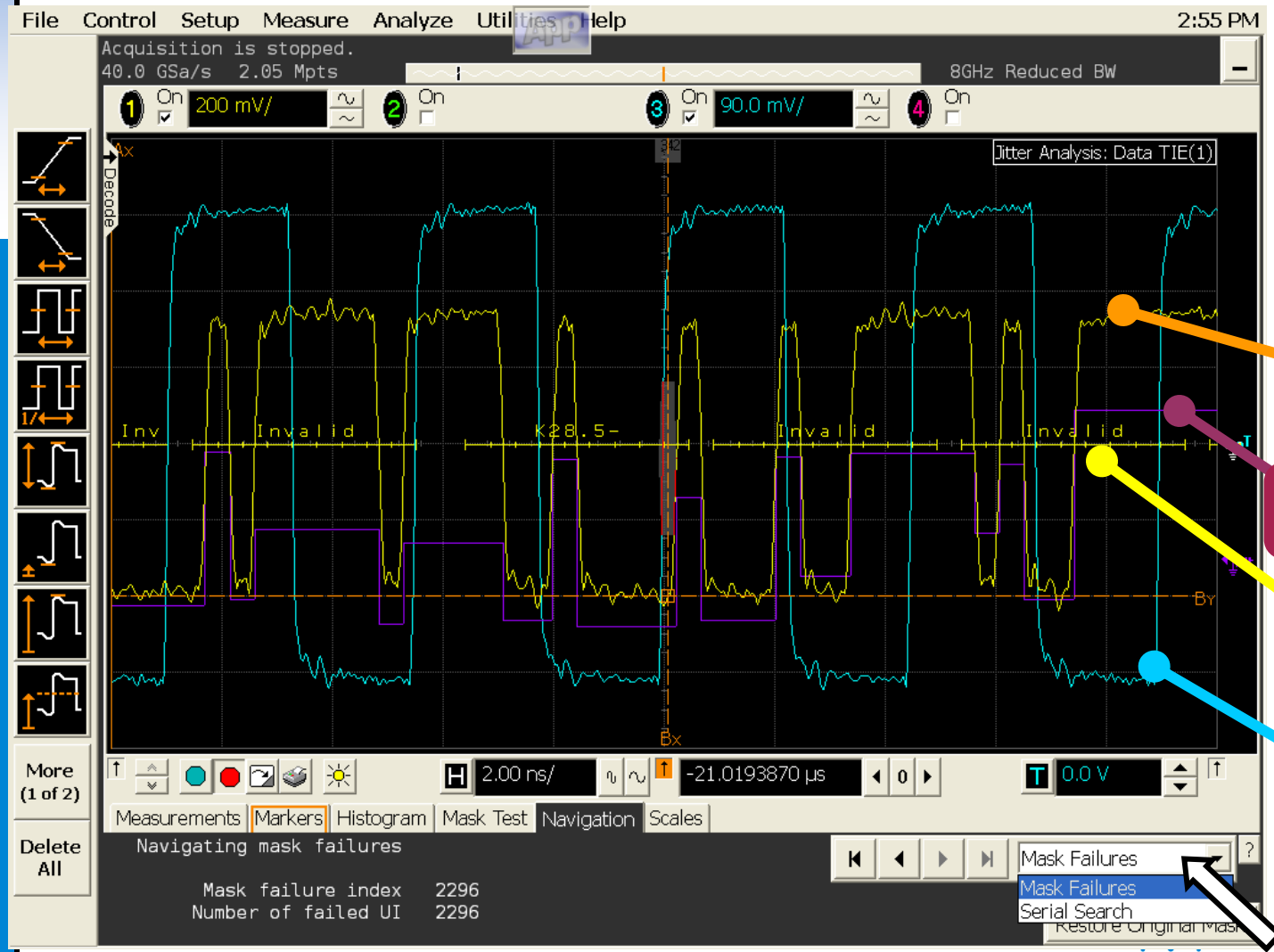
Next Gen Debugging: Infiniium offers *True Seamless Debugging* with All Features Correlating *Simultaneously*



Infiniium even supports "8b10b decodes" on top of other analysis features simultaneously.

CH1:DATA

TIE Jitter Trend

8b10bDecode

CH3:CLK

CLICK !!

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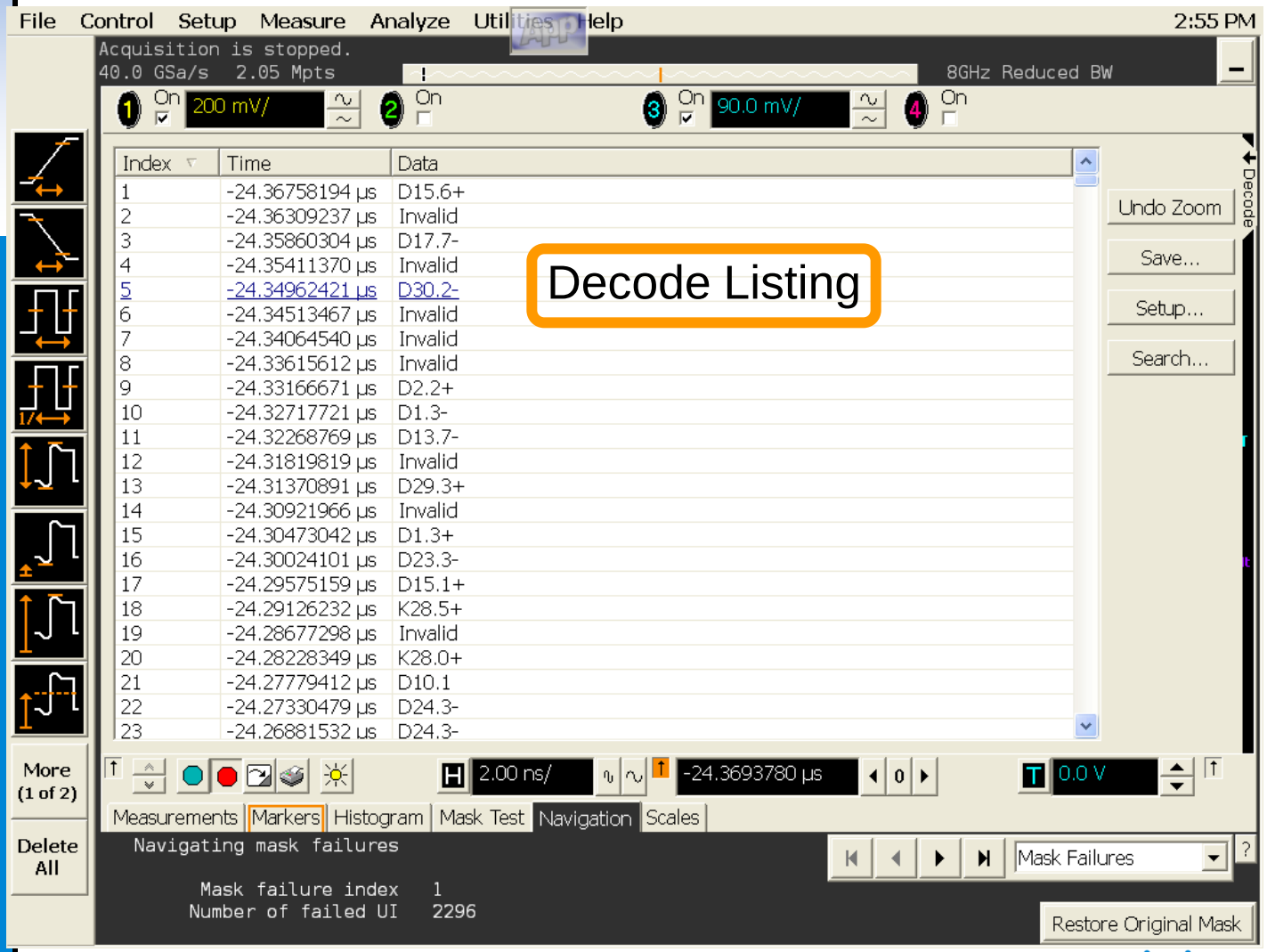
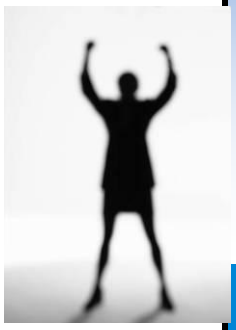
Can your debugging tool work this *seamlessly?*

Next Gen Debugging:
Needless to Say, It Supports the "Decode Listing" as Well





Multi-channel decodes and listing is supported, too!

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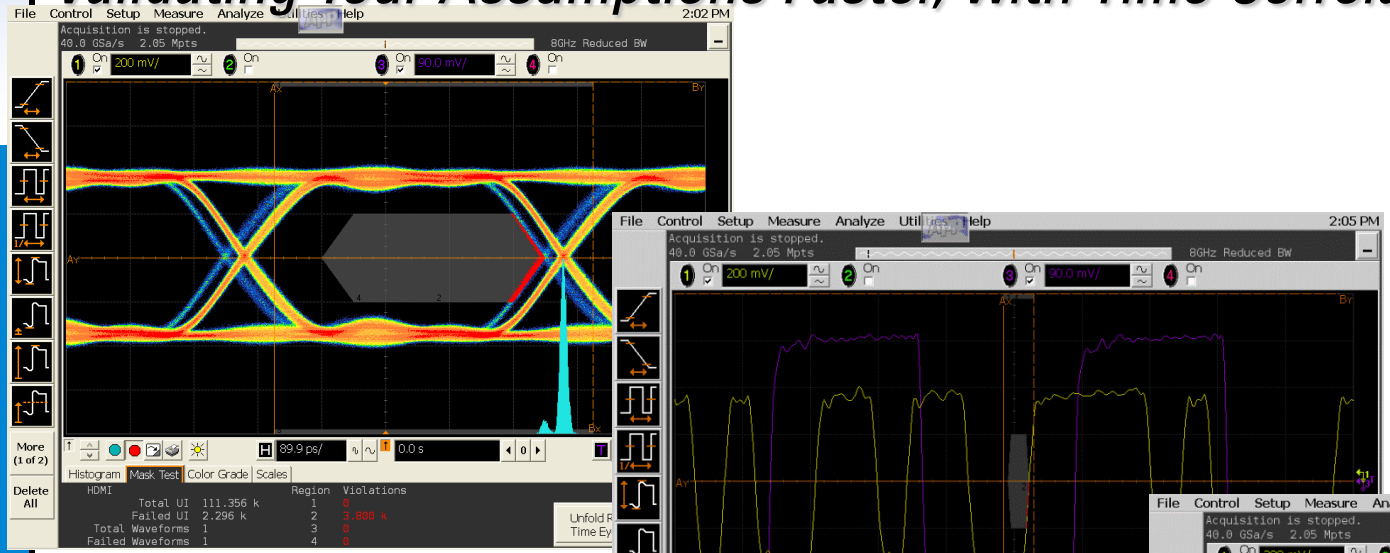
Only the "seamless" debugging tool can realize the ideal debugging solution

Next Gen *Seamless* Debugging is:

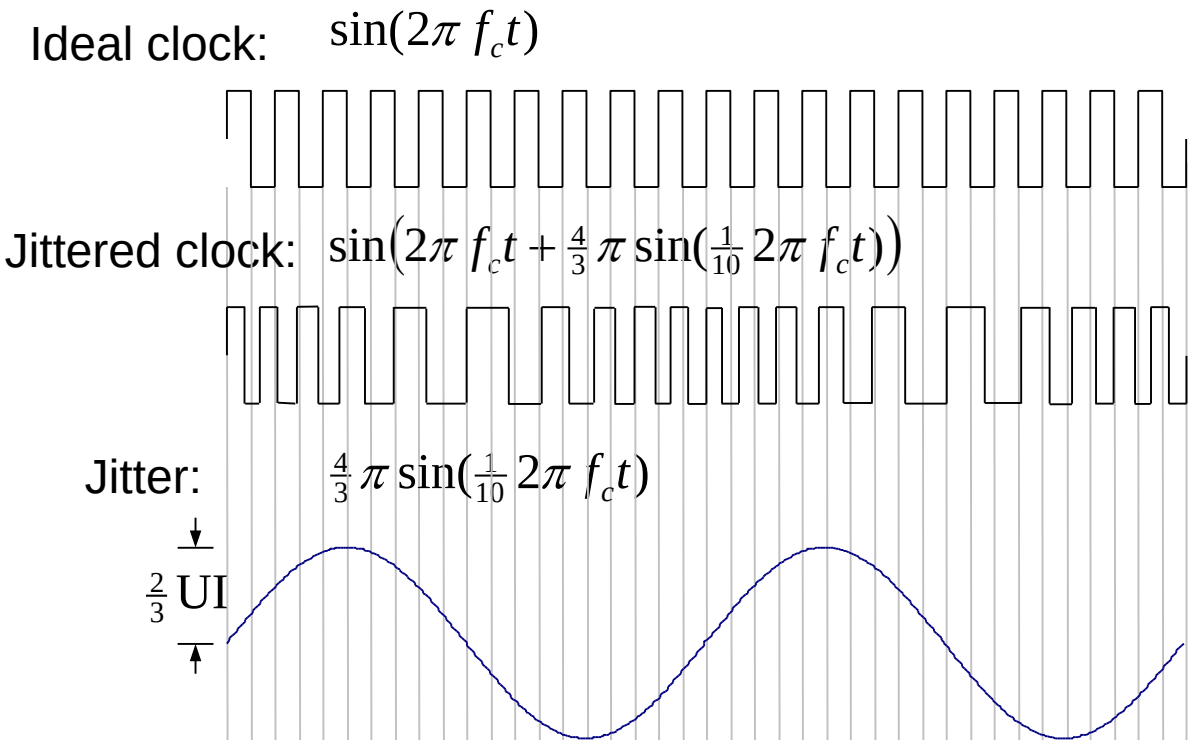
Multi-Perspective Signal Analysis, Getting More Insights Faster, Validating Your Assumptions Faster, with Time Correlating Data



Infiniium will show not only the analysis result, but the cause for the failure.
This is the ***next generation seamless debugging solution***.

What is Jitter?

Jitter is the deviation of a timing event of a signal from its ideal position.



This is the traditional description of jitter,
commonly referred to Time Interval Error (TIE), or phase error.

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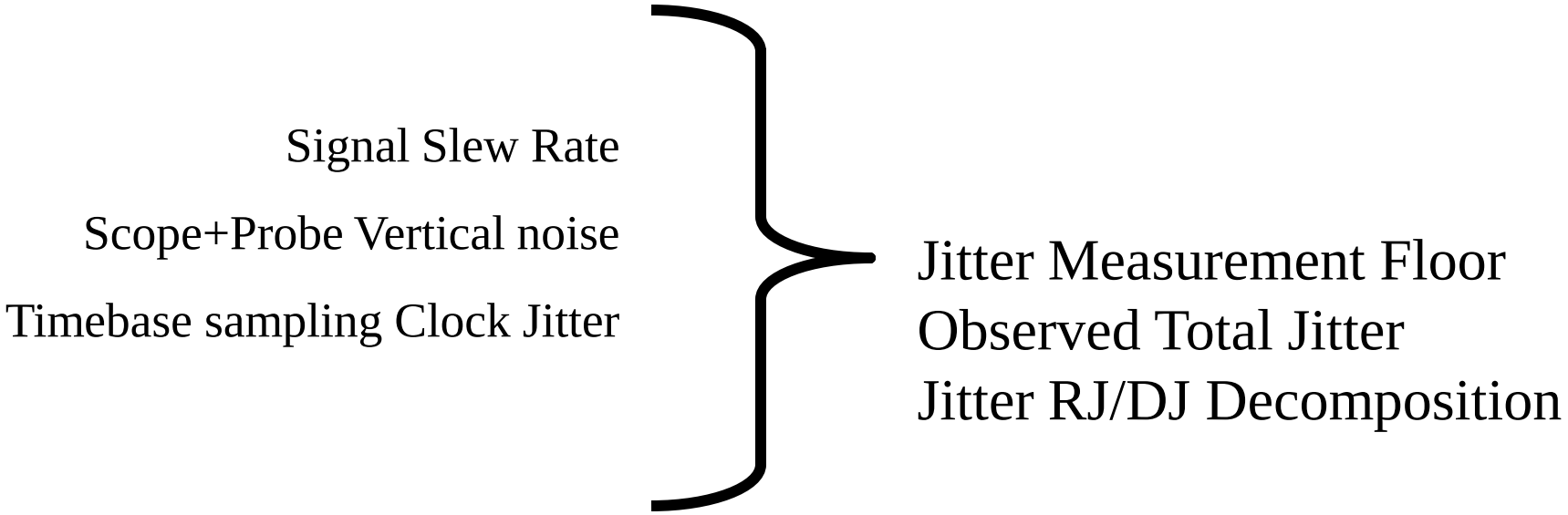
Measuring Jitter with an Oscilloscope



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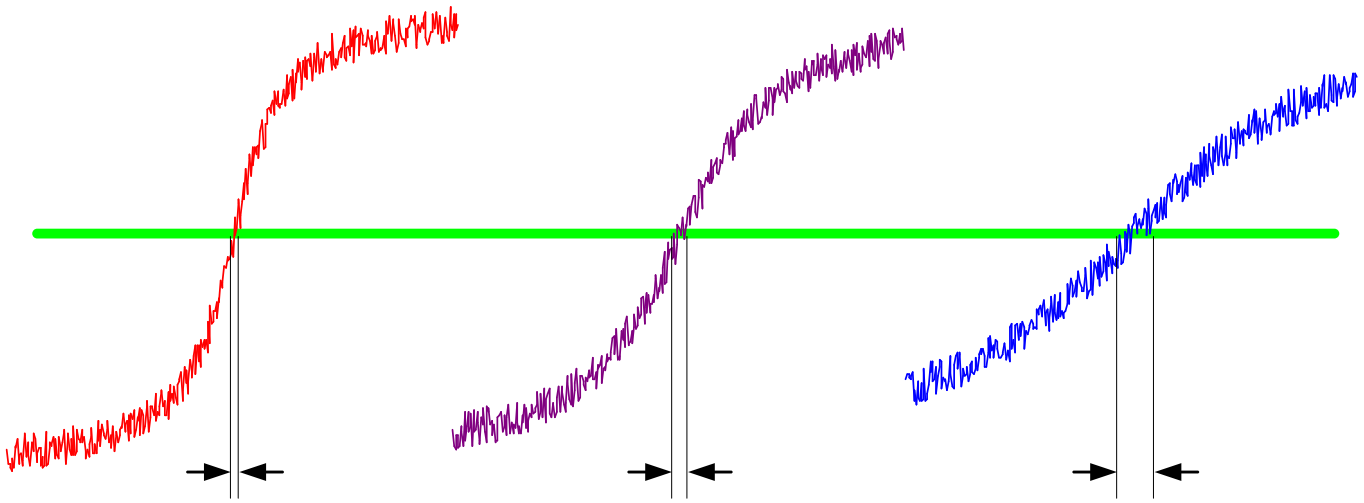
Why is Vertical Noise Floor Important ?

Let's consider a theoretical signals with Zero jitter, fixed voltage noise presenting three different edge speed and crossing a Threshold at 50%



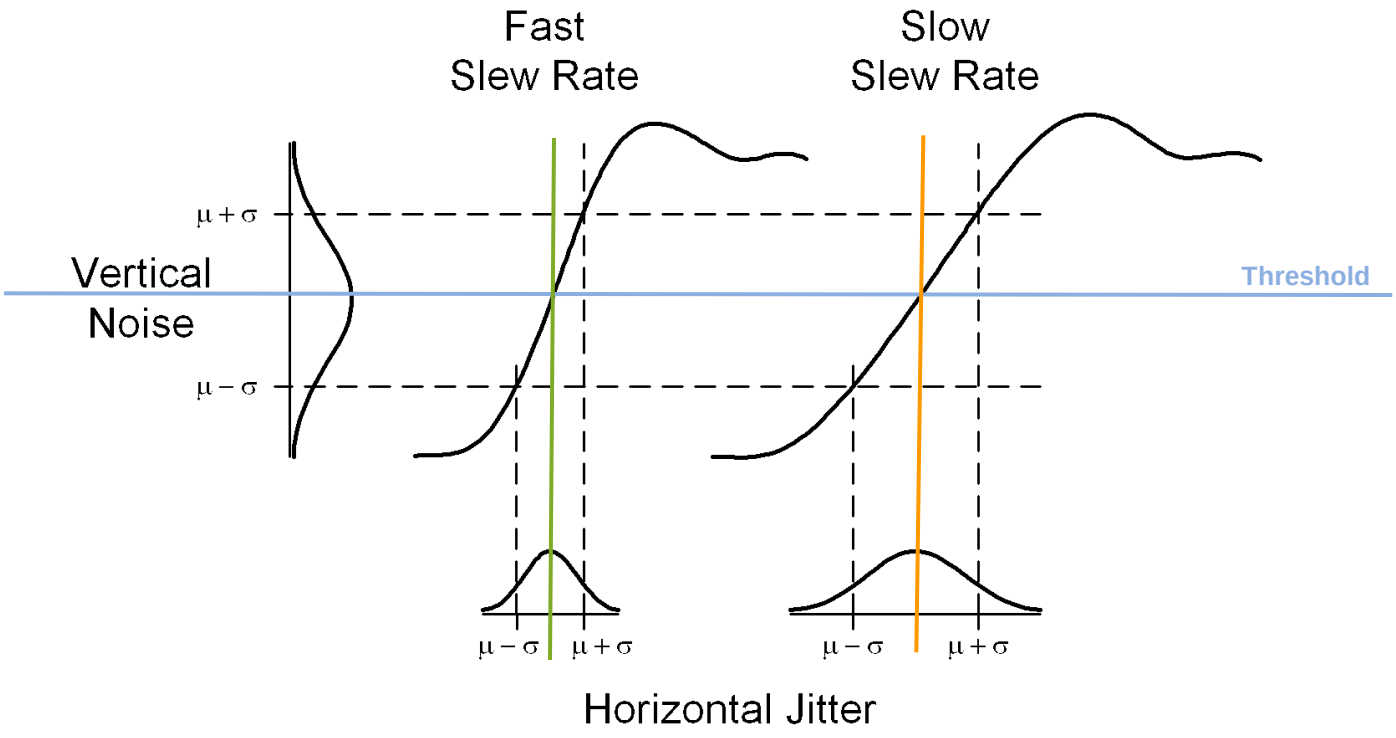
1)Voltage noise translate directly in Timing Uncertainty (also known as Jitter)

2)Higher Vertical Noise Floor translate in Higher Timing Uncertainty

3)At constant amplitude noise floor,
Slower Edge Speed translate into Higher Timing Uncertainty

Some important issues for jitter

- **Measurement accuracy depends on slew rate.**



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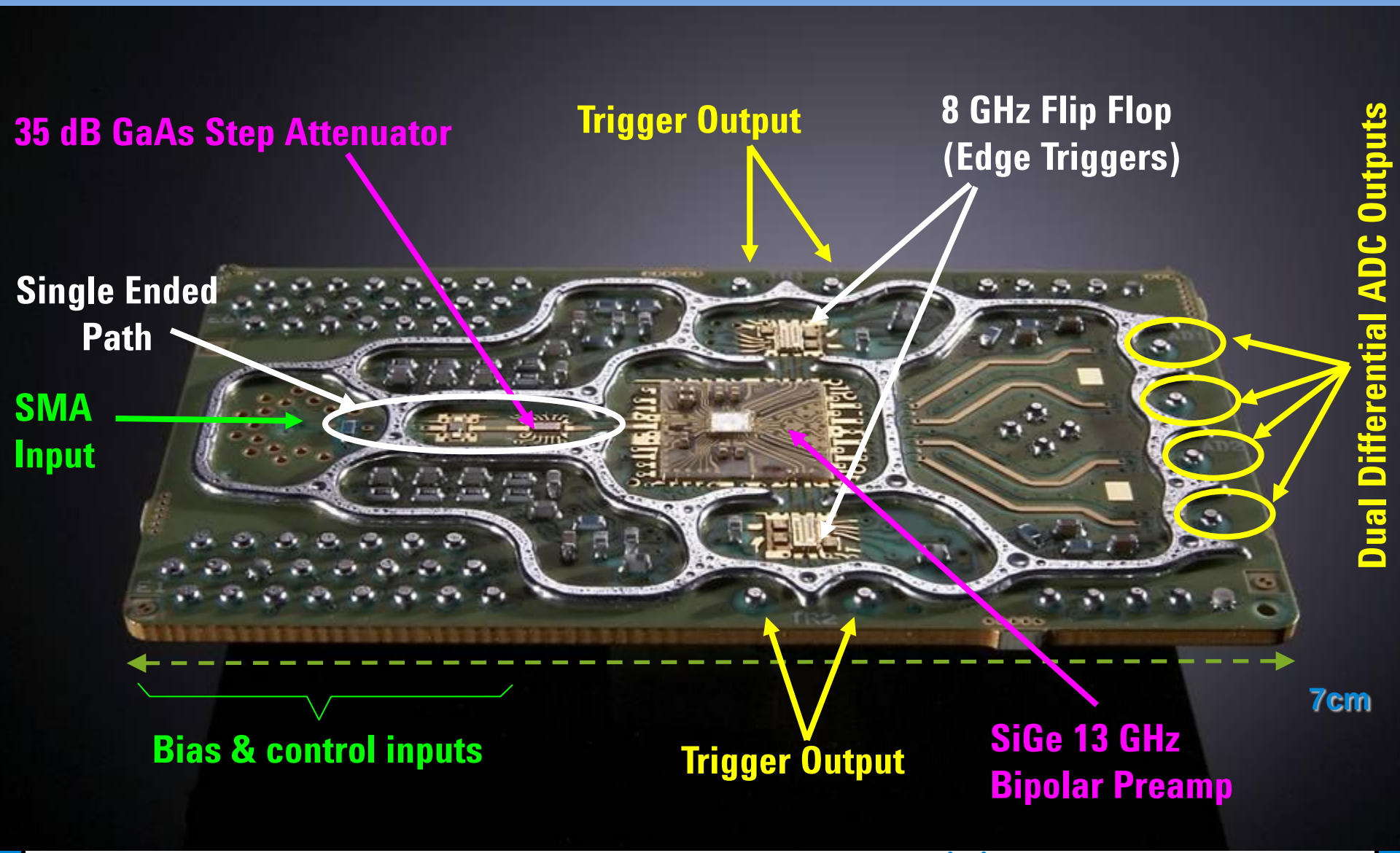
Secret 1 to Infiniium DSO/DSA90000A Series Signal Integrity
The Analog Front End = The MCM (Multi Chip Module)



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System Bandwidth & Noise Floor Considerations

Oscilloscope measurement noise floor is linked to the Bandwidth And Sensitivity setting used

RMS noise floor (scope only)

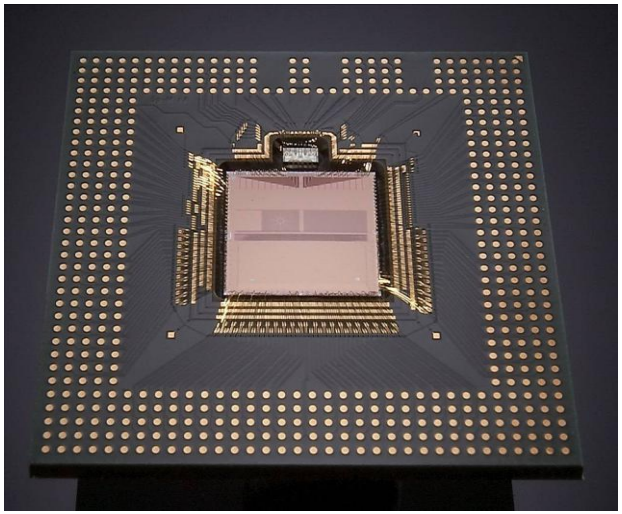
Volts/div	90254A	90404A	90604A	90804A	91204A	91304A
5 mV	153 µV	199 µV	259 µV	322 µV	435 µV	467 µV
10 mV	183 µV	232 µV	295 µV	358 µV	483 µV	536 µV
20 mV	275 µV	342 µV	424 µV	498 µV	650 µV	758 µV
50 mV	645 µV	799 µV	985 µV	1.15 mV	1.45 mV	1.73 mV
100 mV	1.27 mV	1.56 mV	1.92 mV	2.22 mV	2.80 mV	3.37 mV
200 mV	2.47 mV	3.03 mV	3.71 mV	4.28 mV	5.41 mV	6.58 mV
500 mV	6.48 mV	8.00 mV	9.91 mV	11.5 mV	14.7 mV	17.4 mV
1 V	12.5 mV	15.6 mV	19.2 mV	22.3 mV	28.5 mV	34.1 mV

If an active Probe is used, measurement noise increase

RMS noise floor (scope with probe)

Volts/div	90254A with 1131A	90404A with 1132A	90604A with 1134A	90804A with 1168A	91204A with 1169A	91304A with 1169A
20 mV	3.2 mV	3.5 mV	4.0 mV	2.2 mV	2.5 mV	2.7 mV
50 mV	3.3 mV	3.6 mV	4.0 mV	2.3 mV	2.8 mV	3.1 mV
100 mV	3.4 mV	3.8 mV	4.3 mV	2.9 mV	3.5 mV	4.2 mV
200 mV	4.0 mV	4.6 mV	5.3 mV	4.7 mV	5.9 mV	7.5 mV
500 mV	7.1 mV	8.6 mV	10 mV	12 mV	15 mV	19 mV
1 V	13 mV	16 mV	19 mV	23 mV	28 mV	37 mV

Secret 2 to Infiniium DSO/DSA90000A Series Signal Integrity
World First 20GSa/s Single Chip CMOS Analog to Digital Converter



Analog signal goes through a SiGe sample and hold circuit, and is distributed to 80 primary ADCs cell working at 250MSa/s.

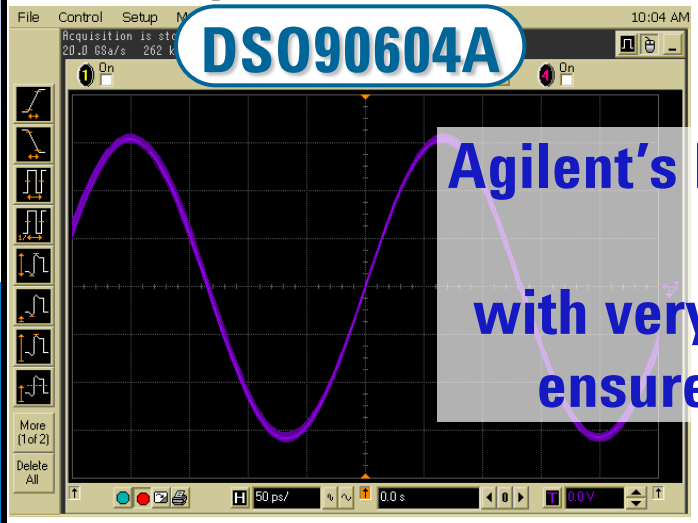
Sampling Clock from Acquisition Board is internaly Delayed 80X using calibrated delay lines ensure best interleaving accuracy.

Result is best oscilloscope measurement accuracy and repeatability

Best Harmonic Distorsion and Spurious Free Dynamic Range

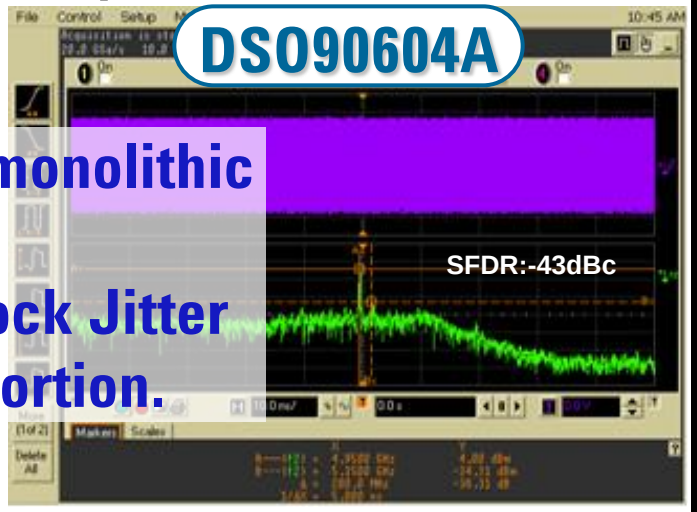
Distortion: Time-Domain Sine Wave Distortion

Input = 3.75GHz Sine Wave 3rd Harmonic of PCI Express 2.5Gb/s



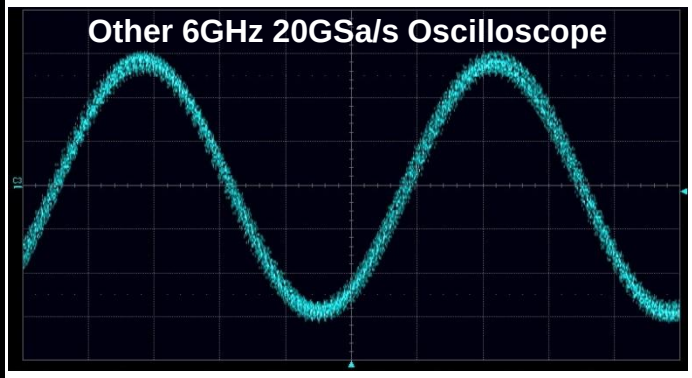
Infinite Persistance Visual Test

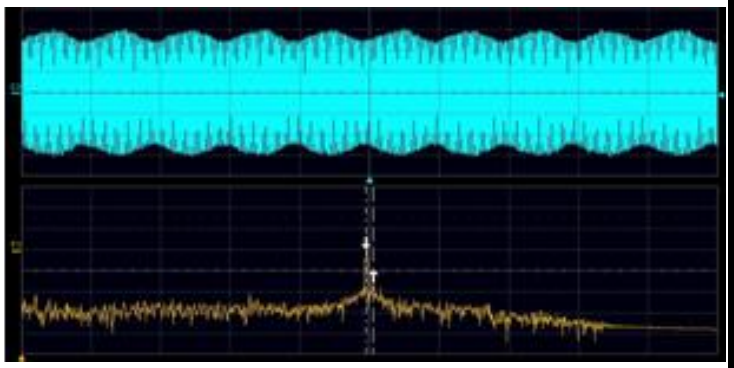
Agilent's highly integrated monolithic 20GS/s ADCs with very low sampling Clock Jitter ensure low levels of distortion.



Slow TimeBase Distorsion

FFT SFDR Measurement





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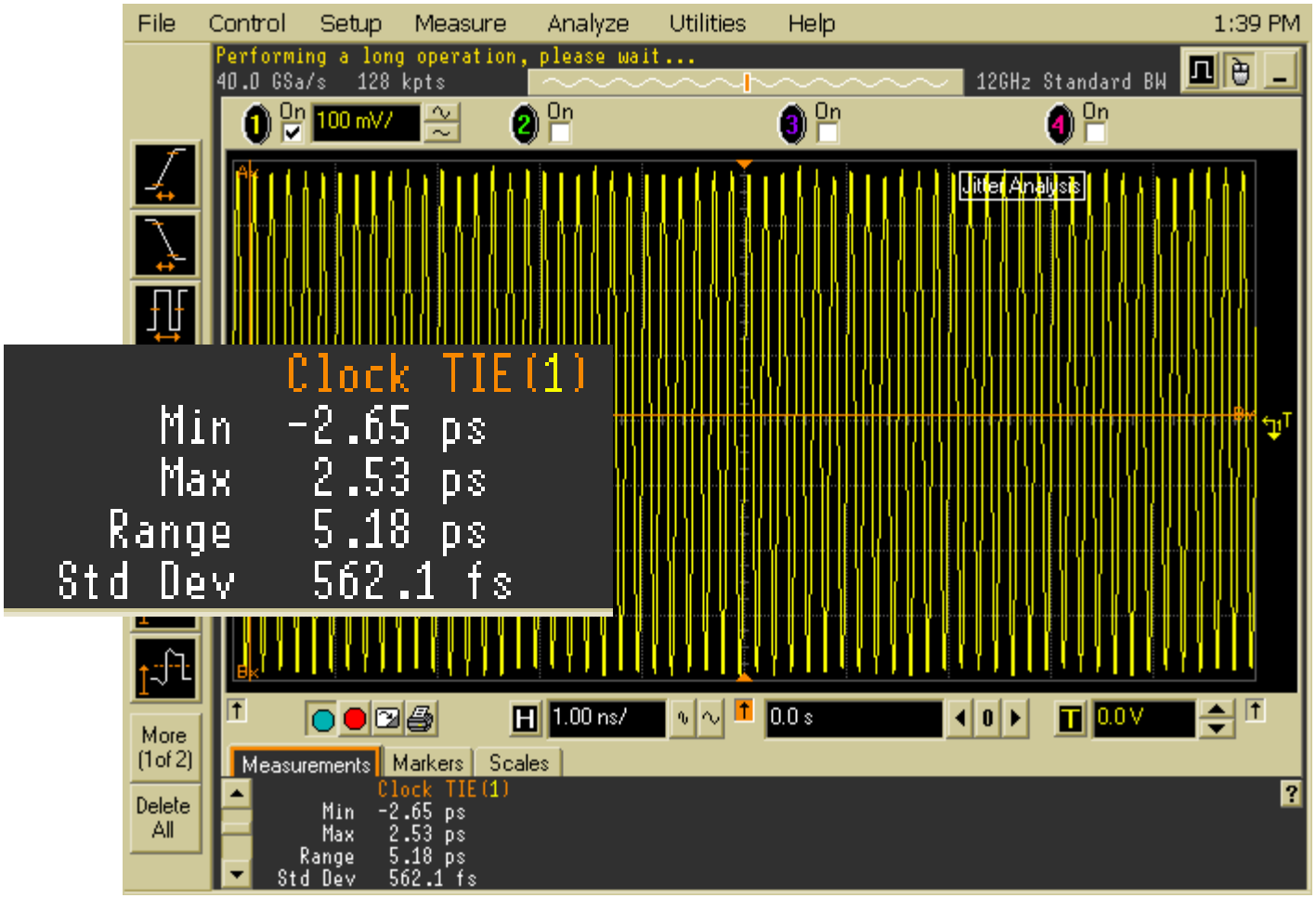
JNF – Best Case



✓**Jitter Noise Floor – 6 GHz sine wave from PSG RF Generator**

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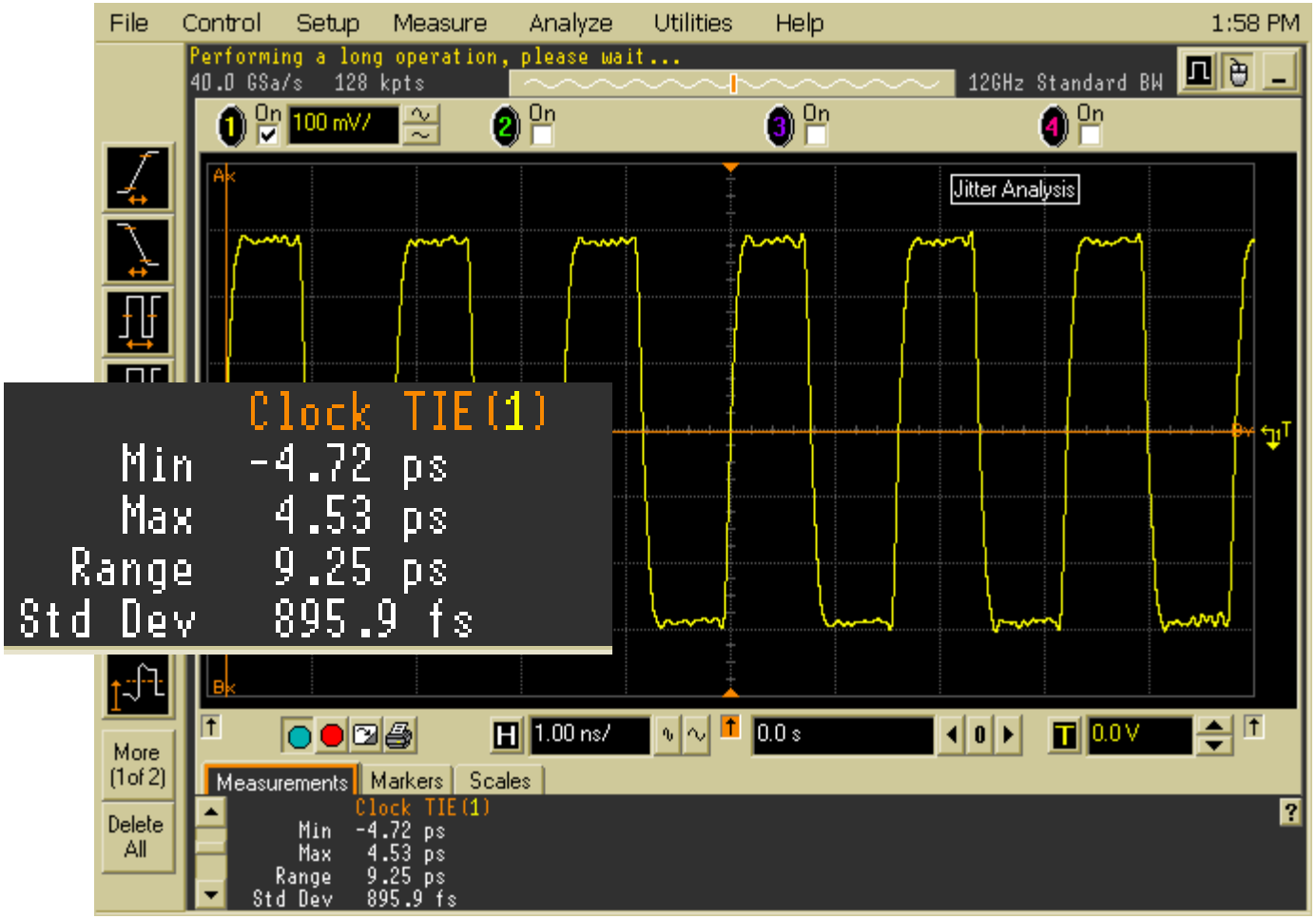
JNF – 150 ps Rise Time



✓**Jitter Noise Floor – 150 ps rise time from N4903A**

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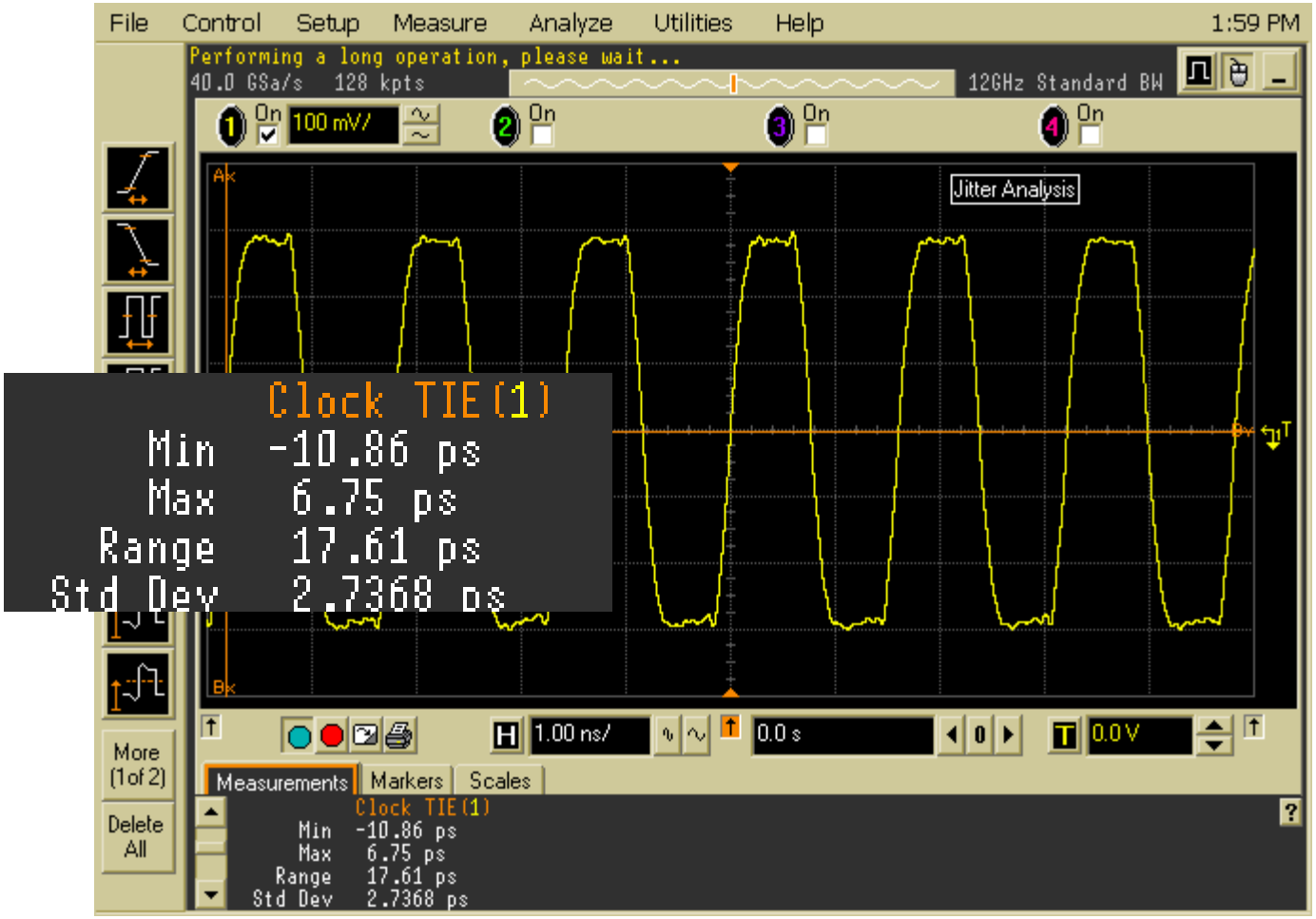
JNF – 250 ps Rise Time



✓Jitter Noise Floor – 250 ps rise time from N4903A

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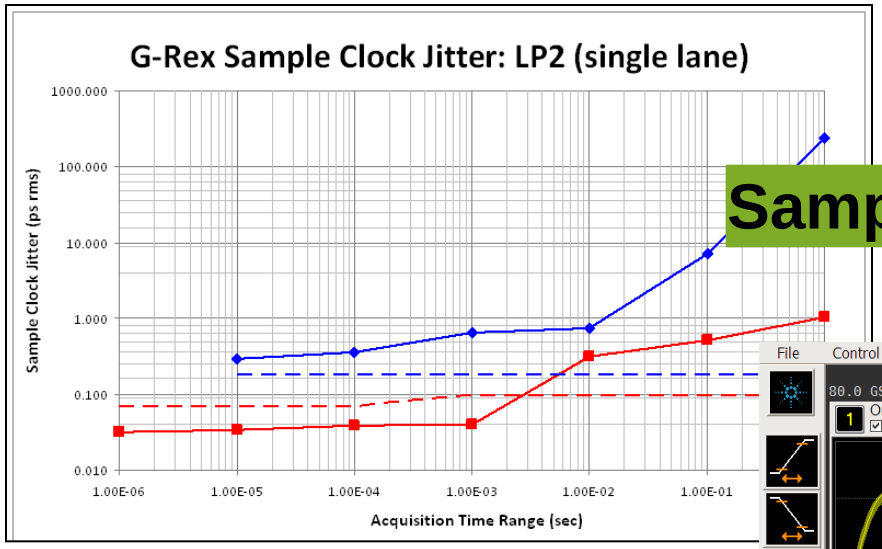
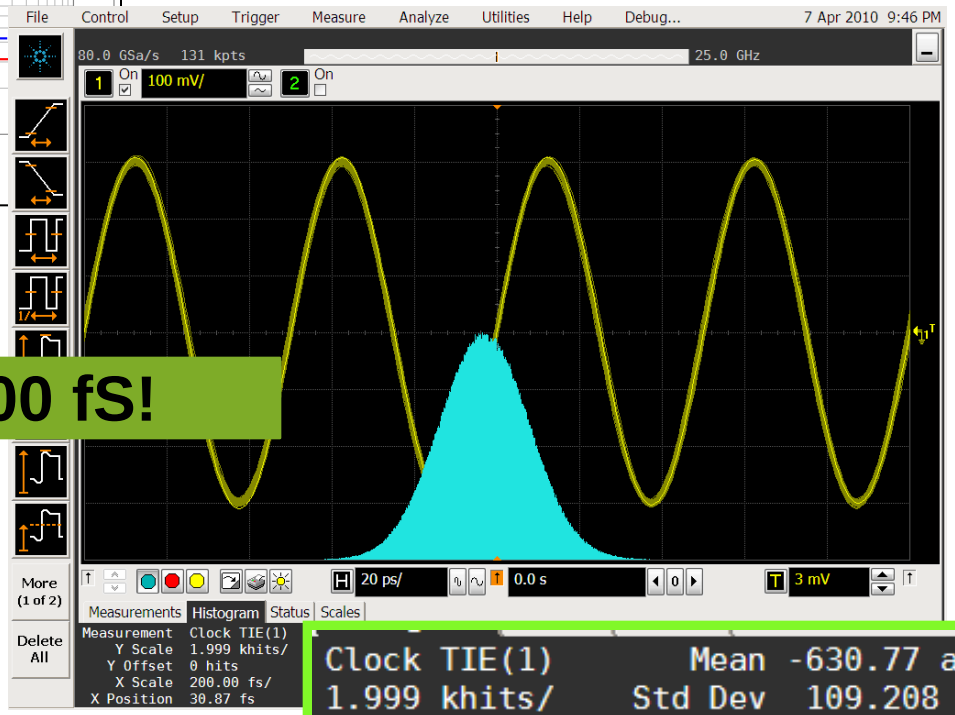
DSOX 903204 True Analog Bandwidth that Delivers

The Industry's Lowest Intrinsic Jitter



Sample Clock Jitter of < 50fS

TIE of 100 fS!



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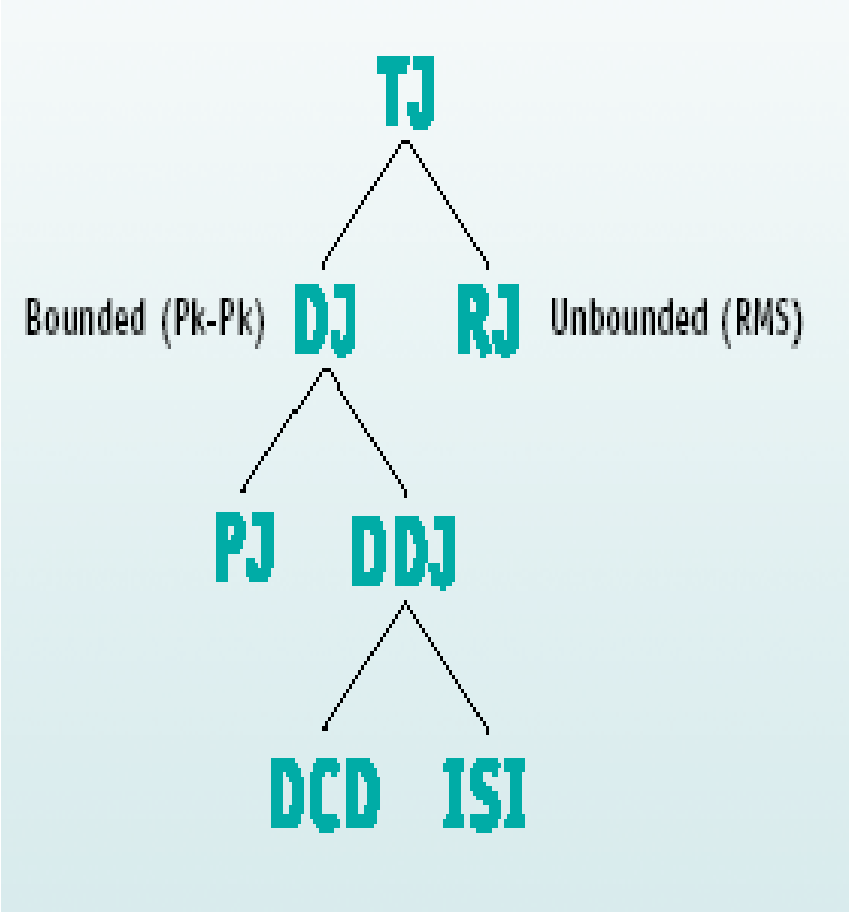
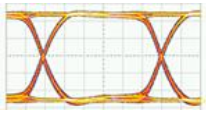
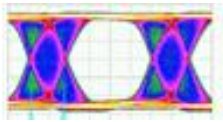
Total Jitter Components



- **TJ: Total Jitter (convolution of RJ (based on BER) & DJ, and measured in peak-to-peak.**
- **RJ: Random Jitter (rms)**
- **DJ: Deterministic Jitter (peak-to-peak).**
  - **PJ: Correlated & uncorrelated Periodic Jitter (caused by cross-talk and EMI)**
  - **DDJ: Data Dependent Jitter**
  - **DCD: Duty Cycle Distortion (caused by threshold offsets and slew rate mismatches).**
  - **ISI: Inter-Symbol Interference (caused by BW limitation and reflections).**

Where Does Jitter Come From?





Transmitter

Receiver

•Lossy interconnect (ISI)
•Impedance mismatches (ISI)
•Crosstalk (PJ)

•Thermal Noise (RJ)
•DutyCycle Distortion (DCD)
•Power Supply Noise (RJ, PJ)
•On chip coupling (PJ, ISI)

•Termination Errors (ISI)

Important settings for accurate results in Eye Diagram & Jitter analysis

- Jitter is measuring timing variation to a reference signal
  - **Clock signal edge position are compared against reference Clock edges**
  - **Data signal edge position are compared against reference Clock edges**

- Is my serial system using an explicit clock I can probe ?
  - **Yes-> Probe the clock and configure scope to use it!**
    - **If receiver apply a multiplier -> scope must be configured to to the same**
    - **If receiver apply a PLL on explicit Clock -> scope must do the same**
  - **No? -> Derive the clock from the data using software PLL emulation**

  - **Software clock recovery must be flexible to imitate Receiver Clock recovery**
  - **Jitter Observed on Oscilloscope depend on Soft PLL Bandwidth Parameter**
  - **Too Big PLL bandwidth transalte into lower observed Jitter**
  - **Too Small PLL bandwidth translate into higher observed Jitter**
  - **The good software PLL BW Value is the one from YOUR Reciever**

What is Real-Time Jitter Analysis?

Real-time jitter analysis consists of a collection of successive timing variation measurements displayed in multiple views where…

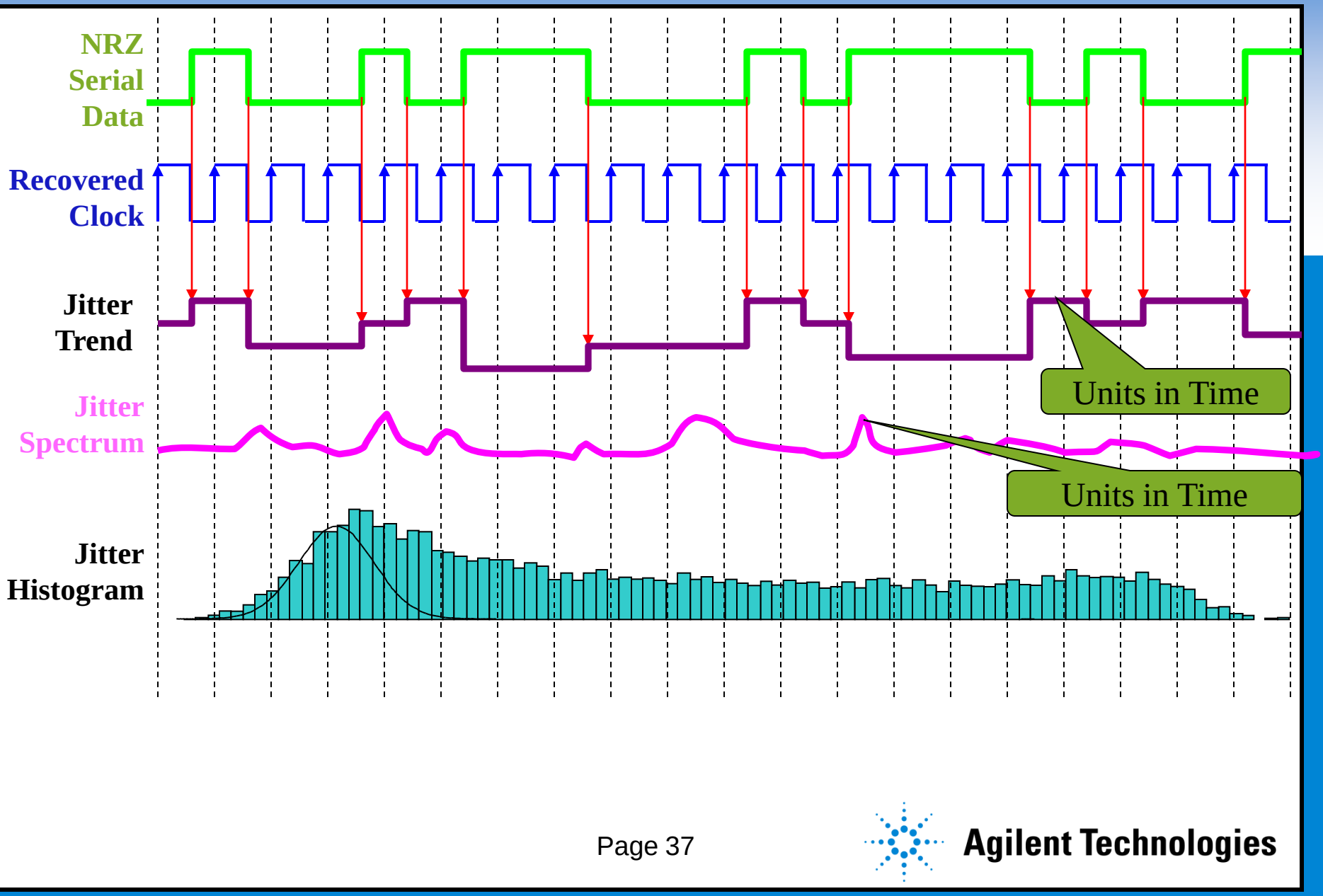
The timing variation measurements can be…

- **Data: Time Interval Error (TIE), sometimes called "phase error"**
- **Clock: Period, Cycle-to-Cycle, N-Cycle**
- **Parametric: Frequency, rise time, setup time, hold time in a synchronous system**

The views includes…

- **Eye Diagrams (repetitive volts vs time)**
- **Histograms (N vs time error)**
- **Trend (time error vs time)**
- **Spectrum (time error vs frequency)**
- **RJ/DJ separation (rms/p-p tabular)**
- **Bathtub curves (BER vs eye opening)**

How Do Real Time Scopes Measure Jitter?



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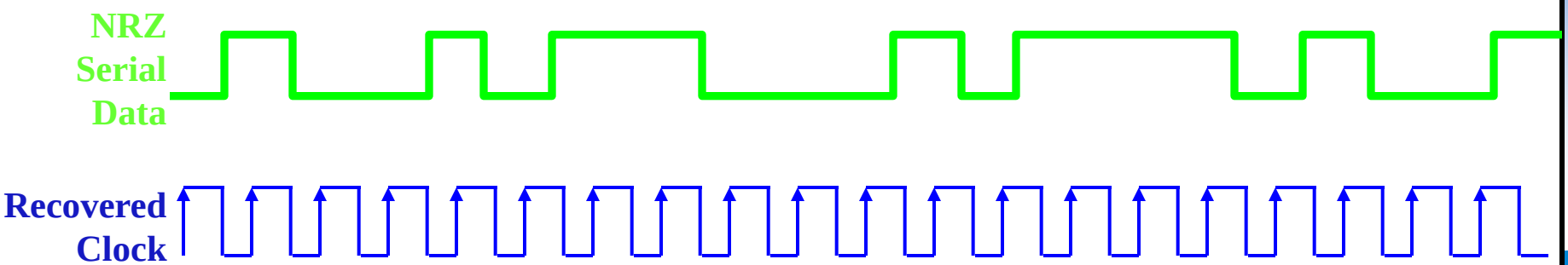
What About Clock Recovery?



Software Clock Recovery

- Low jitter (zero)
- Frequency agile
- Loop BW agile
- Low HW cost (zero)

Hardware Clock Recovery

- Clock is available for other equipment (BERTs, DCAs, etc)
- Required on Sampling Oscilloscopes

Real Time Oscilloscope Trade-offs

Benefits of Real Time Oscilloscope Jitter Measurements

- Can measure jitter frequencies up to 1/2 the data rate
- Can use software for ideal clock recovery (no added jitter)
- Can correlate jitter to other signals (power supply, cross-talk)
- Can measure jitter on live signals with active probes
- General purpose tool, useful for other tasks
- 1 ps rms jitter noise floor typical

Weakness of Real Time Oscilloscope Jitter Measurements

- Measuring low frequency jitter requires lots of Memory
- Limited to data rates < =10 Gb (for now)

Real-time Scope versus Other Jitter Solutions

< 3.2 Gb serial signaling, all synchronous signaling

Compliance
- Component Manufacturers
- 50 ohm fixtured
- Driven by standards work

RT Scopes - Active Probes Needed

Debug
- PCB/System Engineering
- Live Signals
- Logic Analyzers
- Jitter Identification!

Validation
- Probing Sweatshops
- Live Signals
- Ease of use, reliability

BERTs, TIAs, DCAs, Generators

Compliance Testing versus Debugging

Compliance Testing of Components/Sub-systems

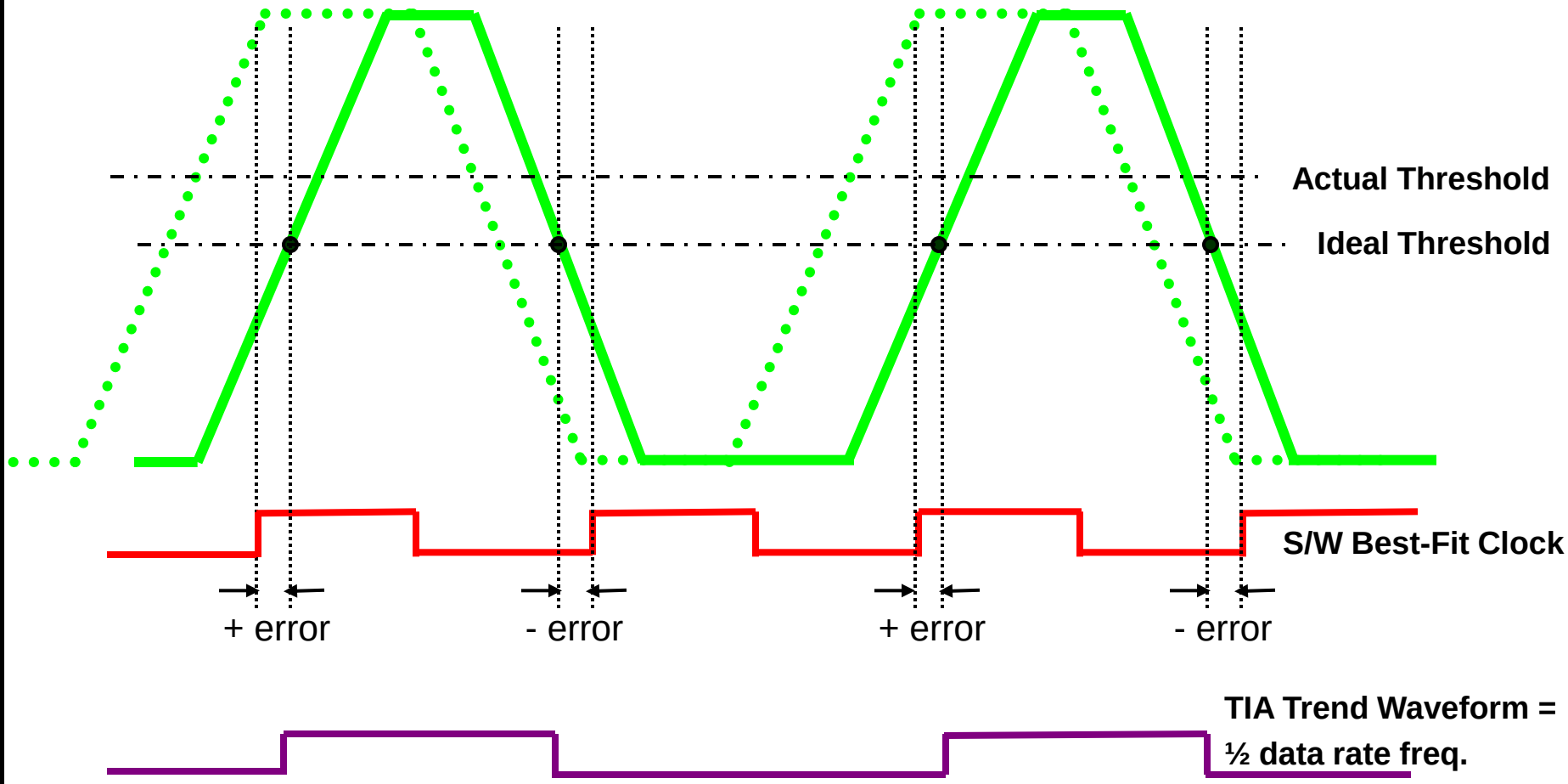
- **Pulse/Pattern Generators used to stimulate "Compliant Jitter Tolerance Patterns (CJTPAT)"**
  - **Ex: 101010… tests for Duty Cycle Distortion (DCD)**
  - **Ex: 1111101010000… tests for Inter Symbol Interference (ISI)**
- **BERTs, TIA's, DCA's, RJ/DJ separation software used to measure/analyze jitter components to meet critical tolerance specifications**

Debugging/Characterization of Systems

- **Real-time Oscilloscopes with Jitter Analysis used to time-correlate sources of jitter within a "live" system at speeds up to 10 Gb/s.**
- **Sampling Oscilloscopes (DCA) with Jitter Analysis use to measure jiiter within a "live" system at speeds greater than 10Gb/s.**

Duty Cycle Distortion (DCD)

Transmitter Threshold Offset Problem



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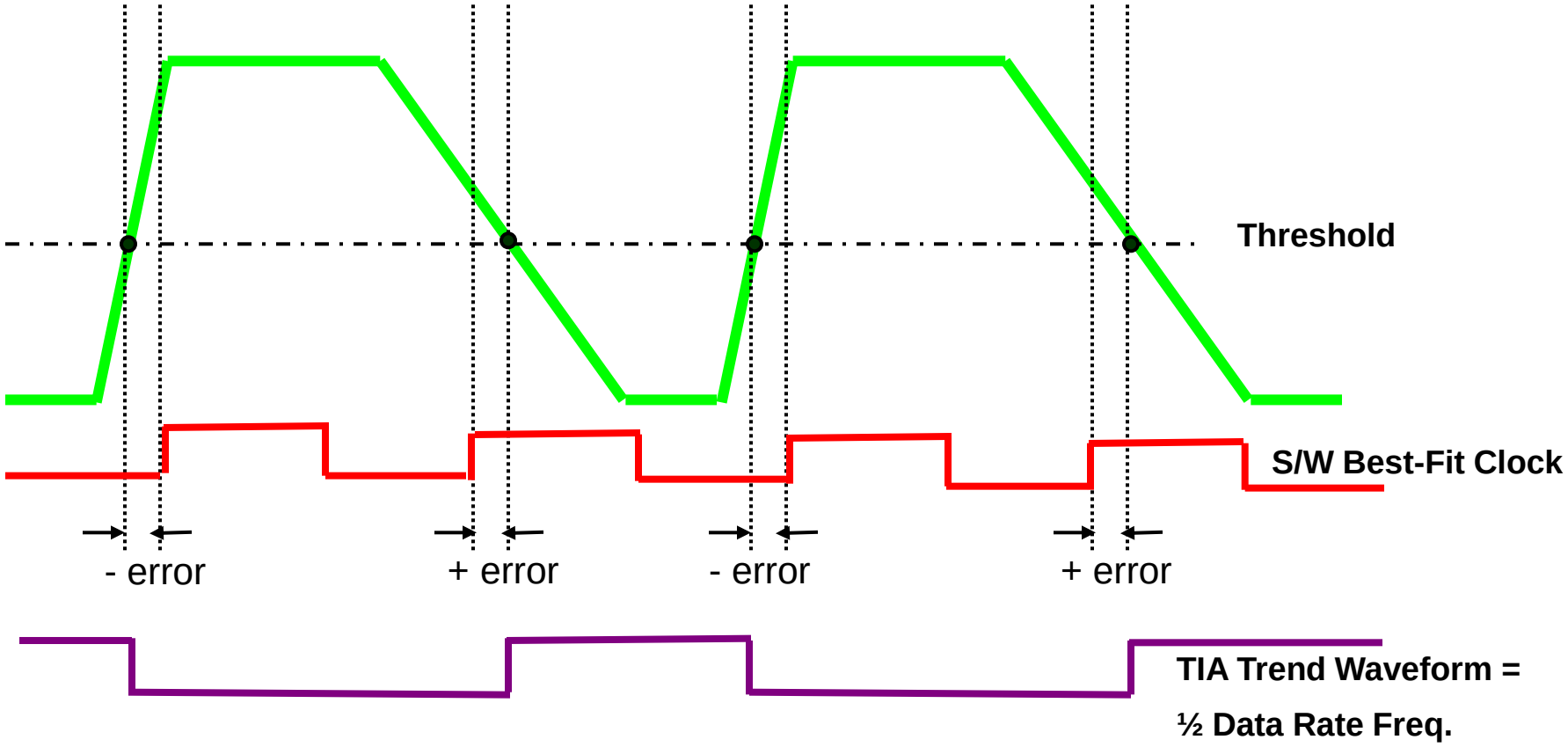
Duty Cycle Distortion (DCD)

Transmitter Edge Transition Speed Mismatch Problem



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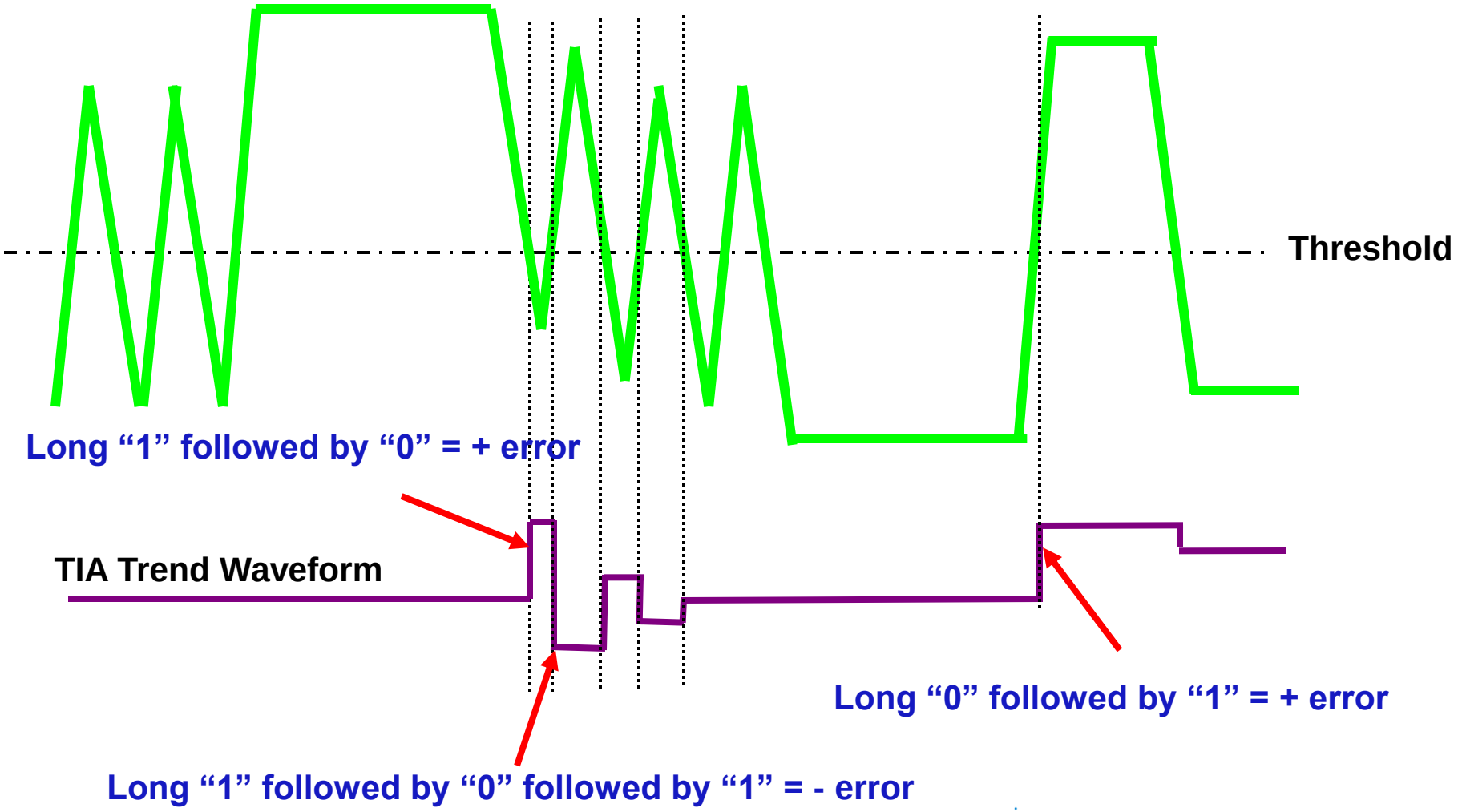
Inter-Symbol Interference (ISI)

Transmission Line Bandwidth Limitation Problem



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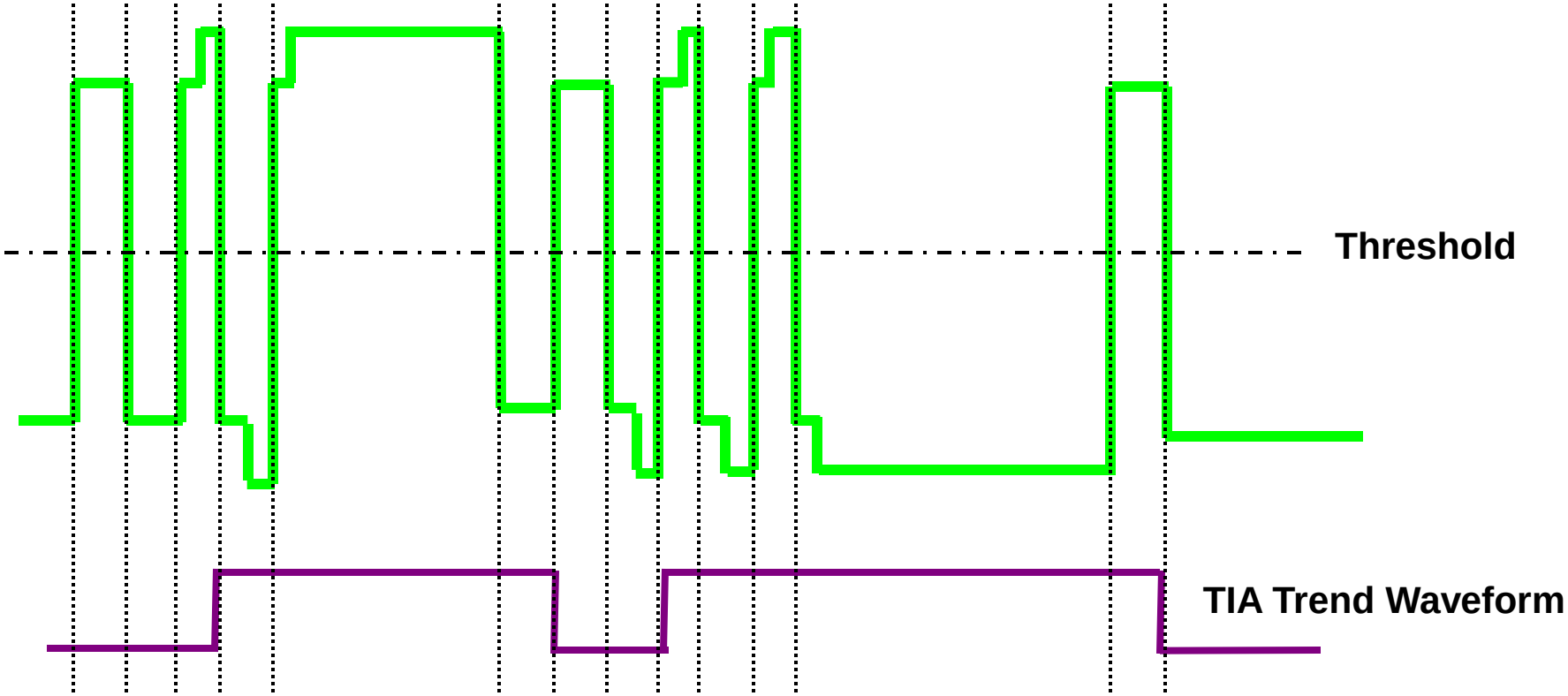
Inter-Symbol Interference (ISI)

Transmission Line Reflection/Improper Termination Problem



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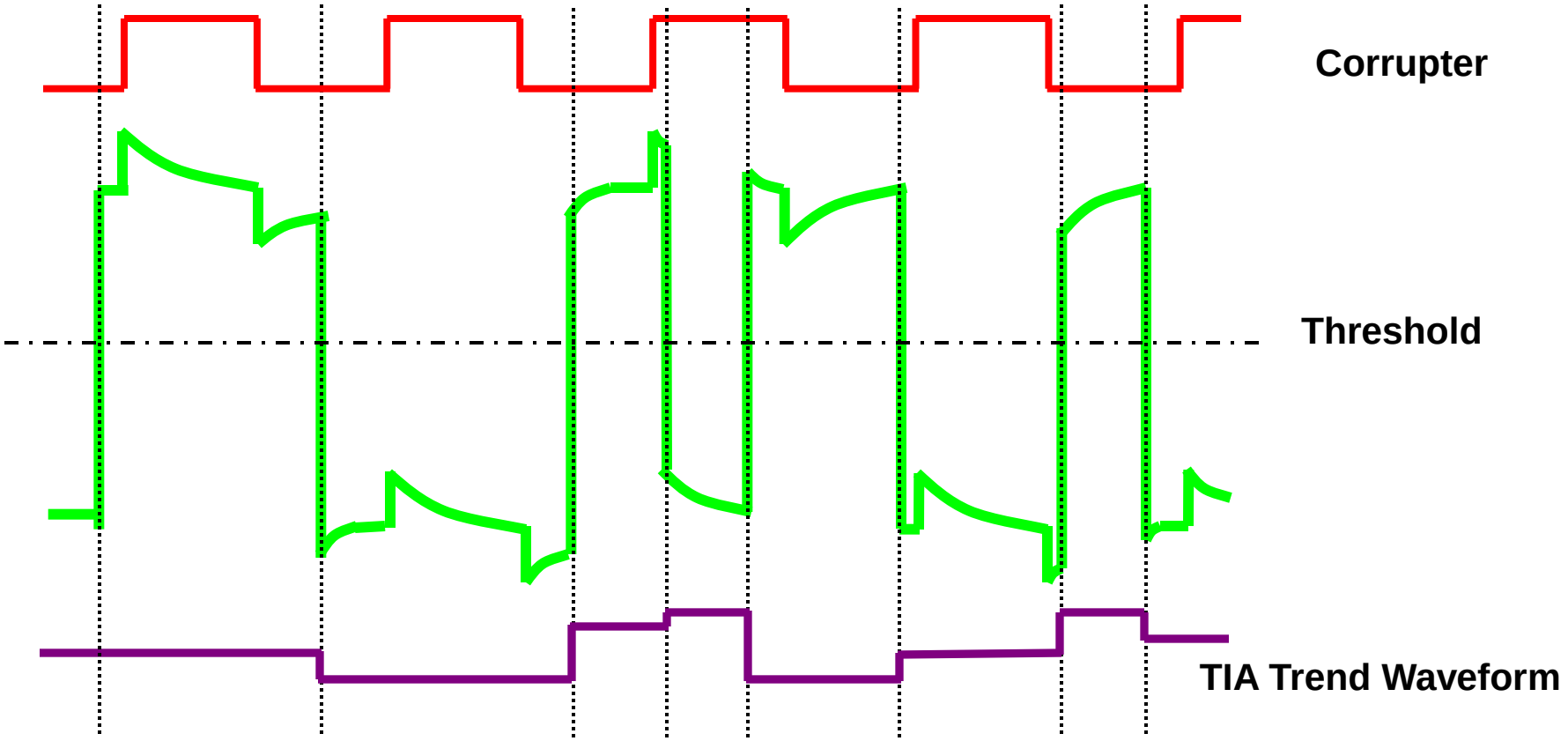
Periodic Jitter (PJ)

System Cross-talk Problem



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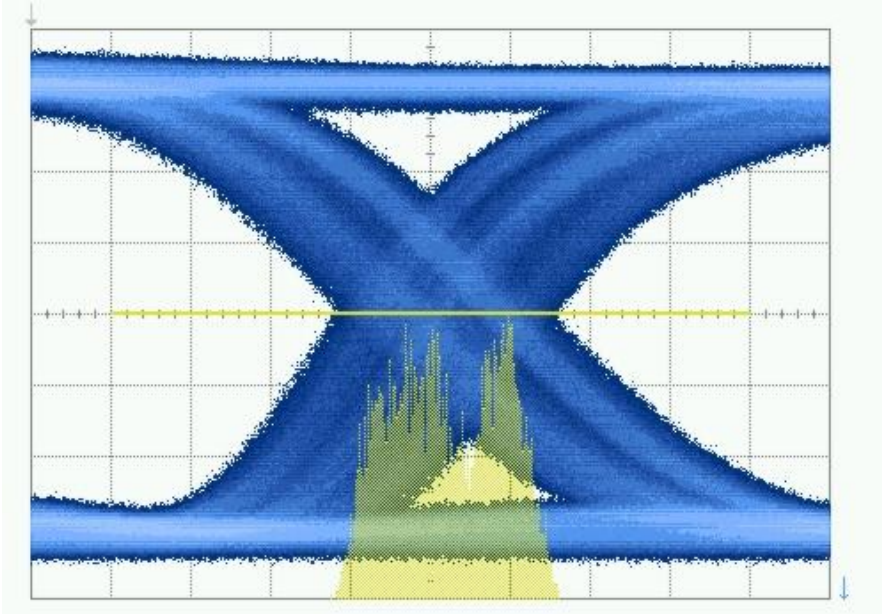
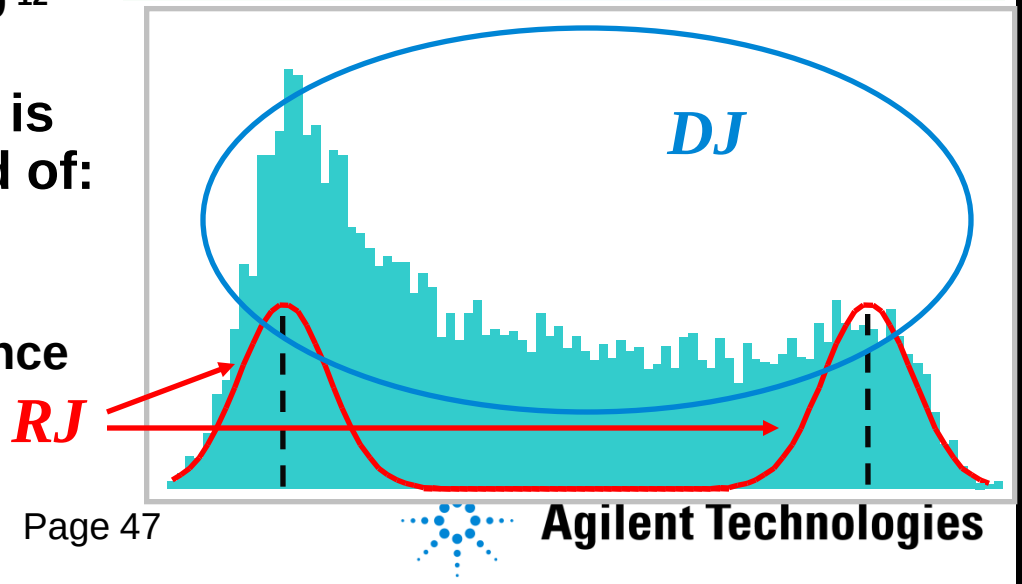
“Real World” Jitter is Complex

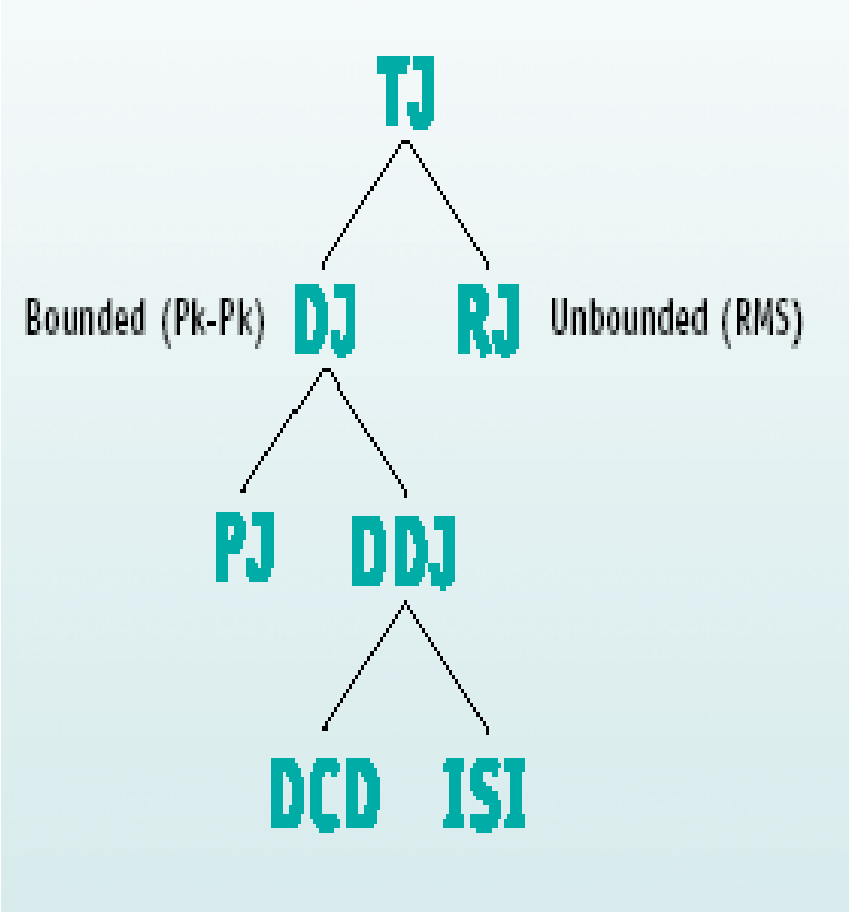
Jitter is composed of both random and deterministic components

- **Random Jitter (RJ) is unbounded**
  - Due to thermal noise, shot noise, etc.
  - Follows a Gaussian distribution
  - Requires a statistical analysis to be quantified
  - RJpp = 14.1 x Jrms for 10^{-12} BER
- **Deterministic Jitter (DJ) is bounded and composed of:**
  - Duty-Cycle-Distortion (DCD)
  - Inter Symbol Interference (ISI)
  - Periodic Jitter (PJ)





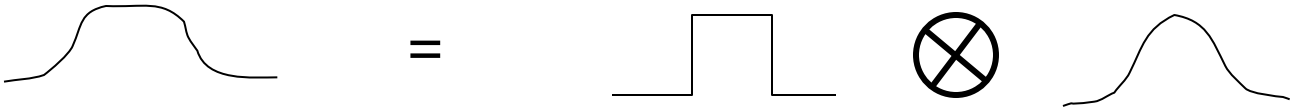
Total Jitter Components



- **TJ: Total Jitter (convolution of RJ (based on BER) & DJ, and measured in peak-to-peak.**
- **RJ: Random Jitter (rms)**
- **DJ: Deterministic Jitter (peak-to-peak).**
  - **PJ: Correlated & uncorrelated Periodic Jitter (caused by cross-talk and EMI)**
  - **DDJ: Data Dependent Jitter**
  - **DCD: Duty Cycle Distortion (caused by threshold offsets and slew rate mismatches).**
  - **ISI: Inter-Symbol Interference (caused by BW limitation and reflections).**

Jitter Probability: BER

$$J_{pk-pk} = J_{deterministic} \otimes n \times \sigma_{random}$$



Bit Error Ratio (BER)	Peak-to-Peak RJ $J_{pp}^{RJ} = n \times \sigma$
10^{-10}	$12.7 \times \sigma$
10^{-11}	$13.4 \times \sigma$
10^{-12}	$14.1 \times \sigma$
10^{-13}	$14.7 \times \sigma$
10^{-14}	$15.3 \times \sigma$

Analysis of Jitter with RealTime Oscilloscope Level One

Realtime Jitter analysis is Key for Debug of Clock and Serial Links

The Jitter Trend (Jitter_amplitude(t))

Probability Distribution Function of Jitter Trend

Standard deviation and Peak to Peak Deviation

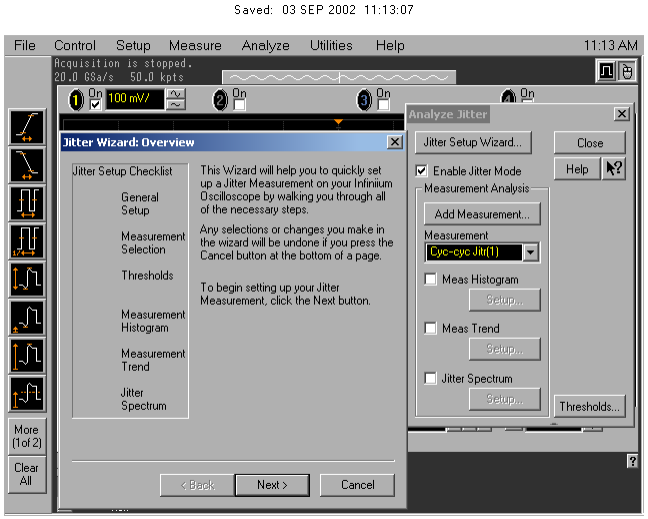
The FFT of the Jitter Trend

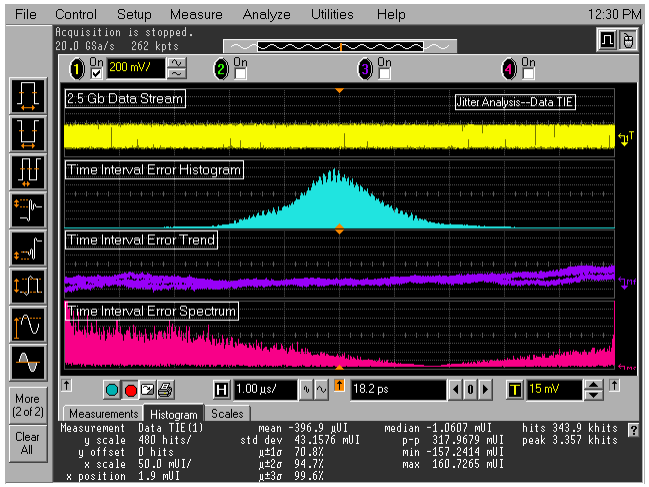
Jitter Trend Shape and FFT content will help establish short of suspects signals on board.

Using a second Channel of Oscilloscope for Trigger, probing suspect signal on board and looking if Jitter Trend spikes/shape is synchronous to probed signal will clearly identify guilty signal.

EZJIT Jitter Analysis Option - Easy to Use

- Key measurements include: cycle-cycle jitter, n-cycle jitter, period jitter, time interval error, setup and hold time, measurement histograms, measurement trending and jitter spectrum.
- Integrated into the oscilloscope application, highly interactive, and time-correlated.
- Setup Wizard guides the user on setup of the jitter measurement, describes what the measurement does and tells you when to use it.





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Agilent EZJIT Jitter Measurement Application

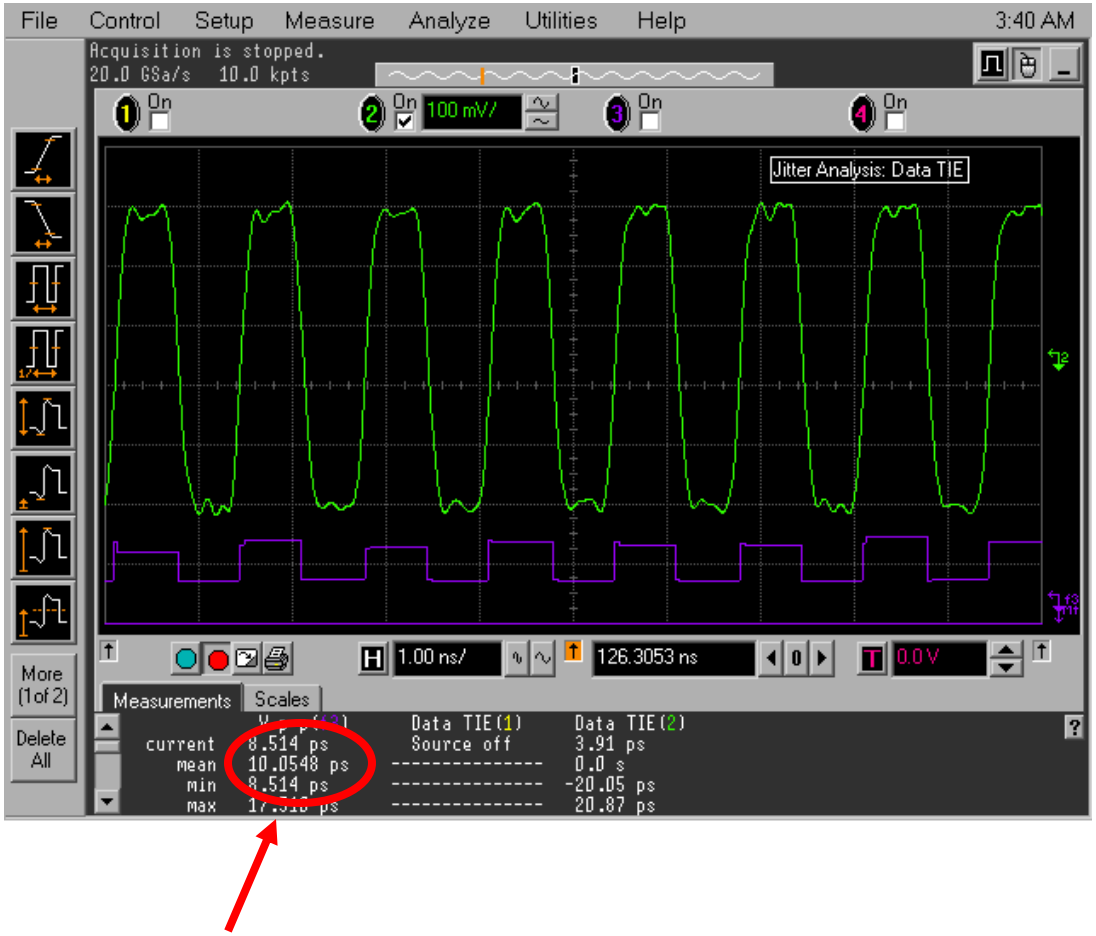
Techniques to Isolate Jitter Components

In the real world, jitter components are NOT isolated

Tools/Techniques used to isolate jitter

- **Serial Pulse/Pattern Generators**
- **Synchronous Triggering**
- **Use of Waveform Math (Averaging, +/-, etc.) on jitter trend results**
- **Fast update rates with real-time time-correlation**
- **TDR**

Duty Cycle Distortion (DCD) Jitter



DCD Jitter (p-p) = 10.05ps

Isolation Technique:

- **Stimulating with slow repeating 1-0-1-0… pattern to eliminate ISI jitter.**
- **Establish a synchronous trigger.**
- **Average trend to eliminate RJ and uncorrelated PJ.**
- **Identified by Trend Waveform @ ½ date rate frequency.**
- **Measure peak-to-peak jitter.**

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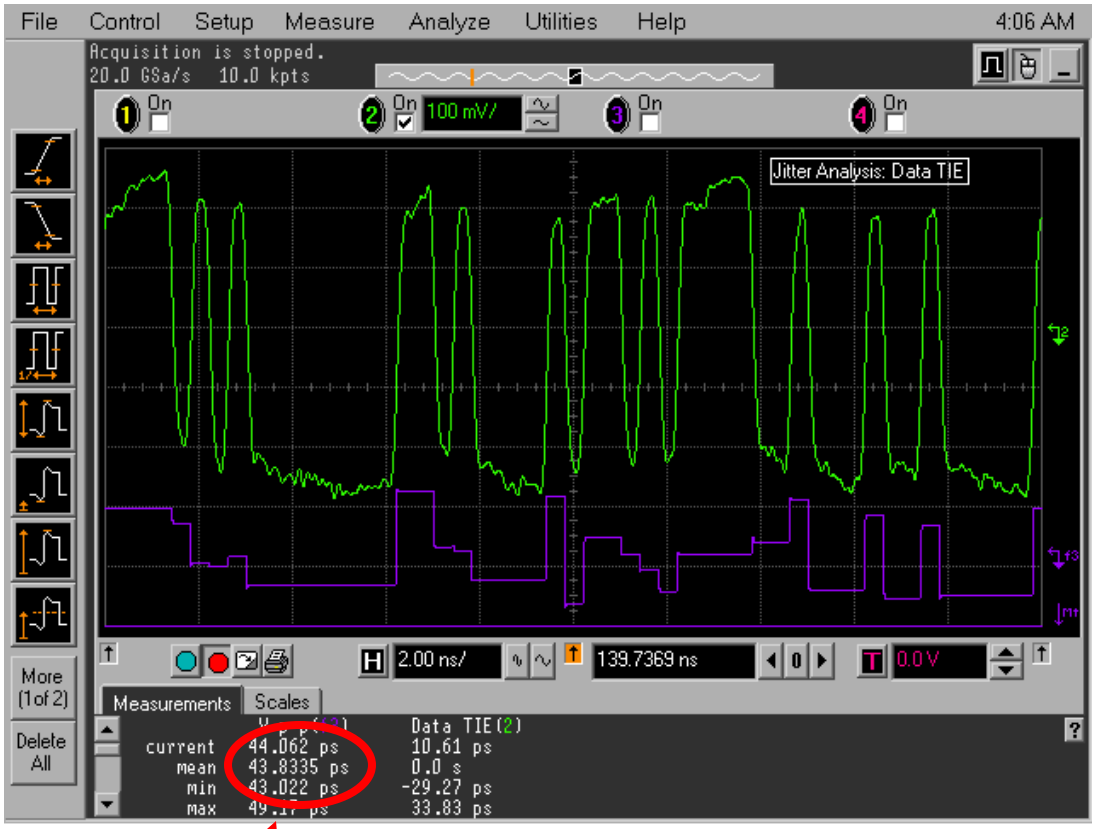
Inter-Symbol Interference (ISI) Jitter due to BW Problem



DCD + ISI Jitter (p-p) = 43.8ps

Note: With known good stimulus source, DCD will be minimal

Isolation Technique:

- **Identified by modulated pulse amplitudes.**
- **With synchronous trigger Average Trend to eliminate RJ and uncorrelated PJ components.**
- **Identified by TIE trend waveform with +error after long 1 or long 0.**
- **Identified by TIE trend waveform with –error after short 1 or short 0.**
- **Measure peak-to-peak.**

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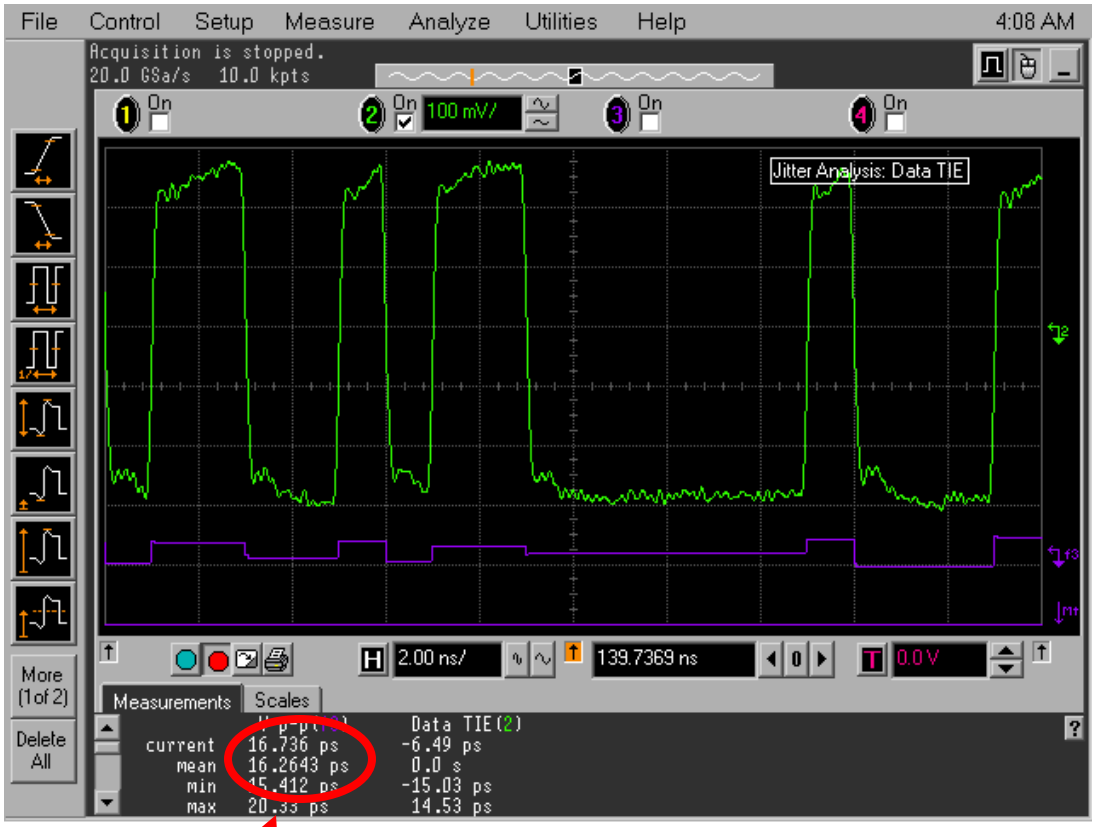
Inter-Symbol Interference (ISI) Jitter due to BW Problem



- **Reduce data rate to test for reduction of ISI component.**
- **DCD and correlated PJ component remains.**
- **Measure peak-to-peak.**

ISI Jitter (p-p) = 16.3ps

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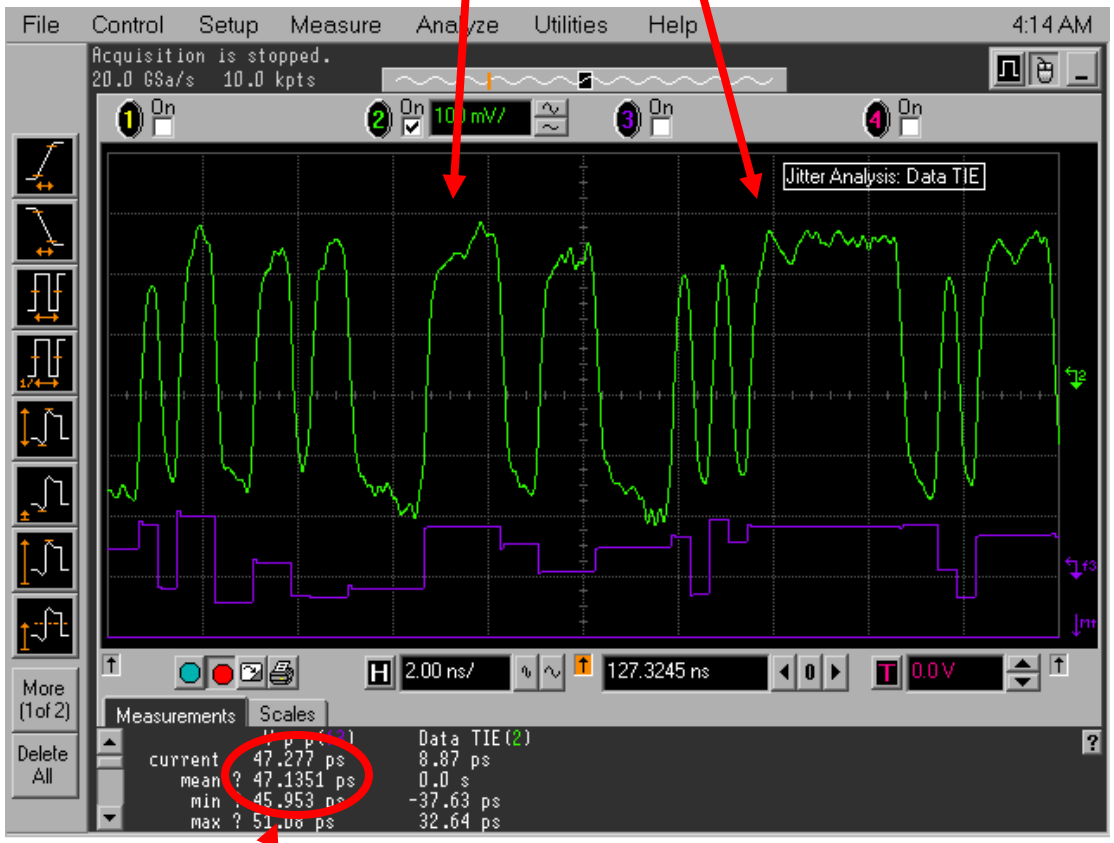
Inter-Symbol Interference (ISI) Jitter due to BW and Reflection Problems

Dissimilar long “1” pulse shapes



- Identified by modulated pulse amplitudes.
- Average Trend to eliminate RJ and uncorrelated PJ.
- Identified by “dissimilar” pulse shapes for long 1’s or long 0’s preceded by dissimilar patterns.

ISI Jitter (p-p) = 47.1ps

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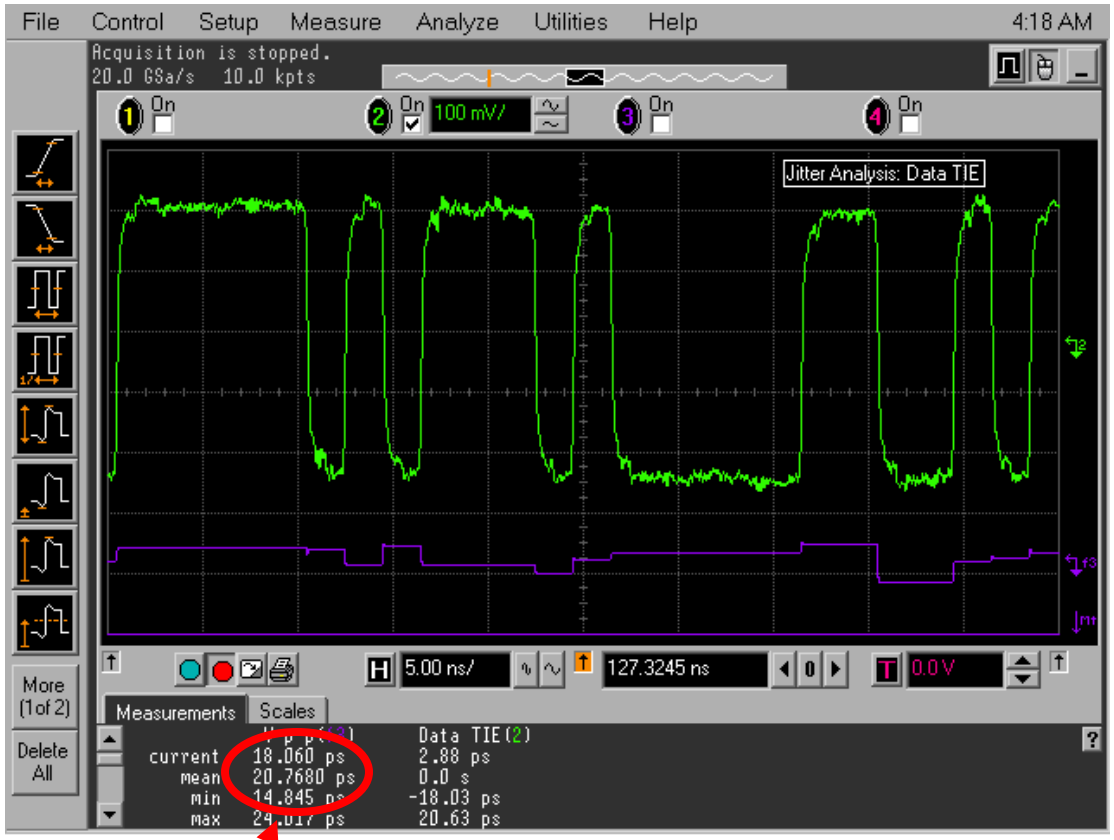
Inter-Symbol Interference (ISI) Jitter due to BW and Reflection Problems



- **Reduce data rate to test for reduction of ISI component at receiver side.**
- **DCD remains.**
- **Measure peak-to-peak.**

ISI Jitter (p-p) = 20.8ps

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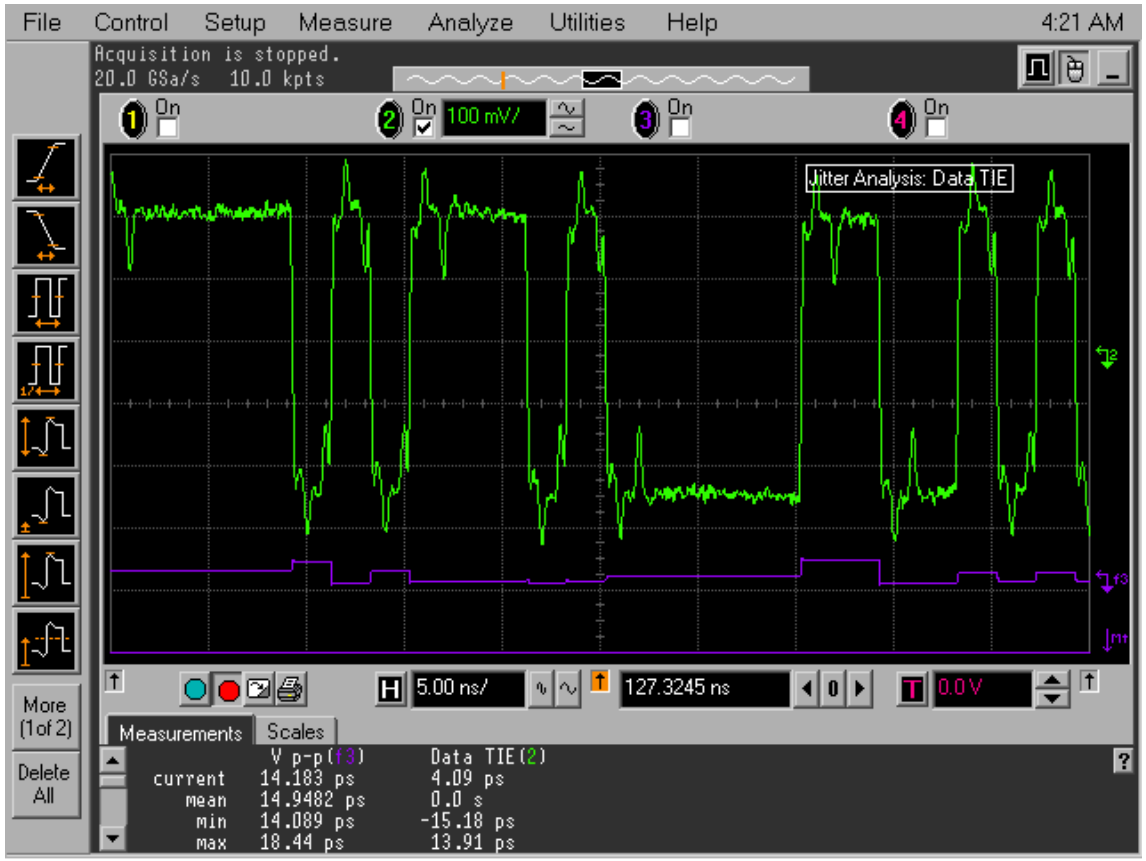
Inter-Symbol Interference (ISI) Jitter due to BW and Reflection Problems



- **Reduced data rate and then capture signal at transmitter side to check for obvious reflections & signal distortions.**
- **Use TDR to accurately characterize transmission line for impedances and distances to anomalies.**

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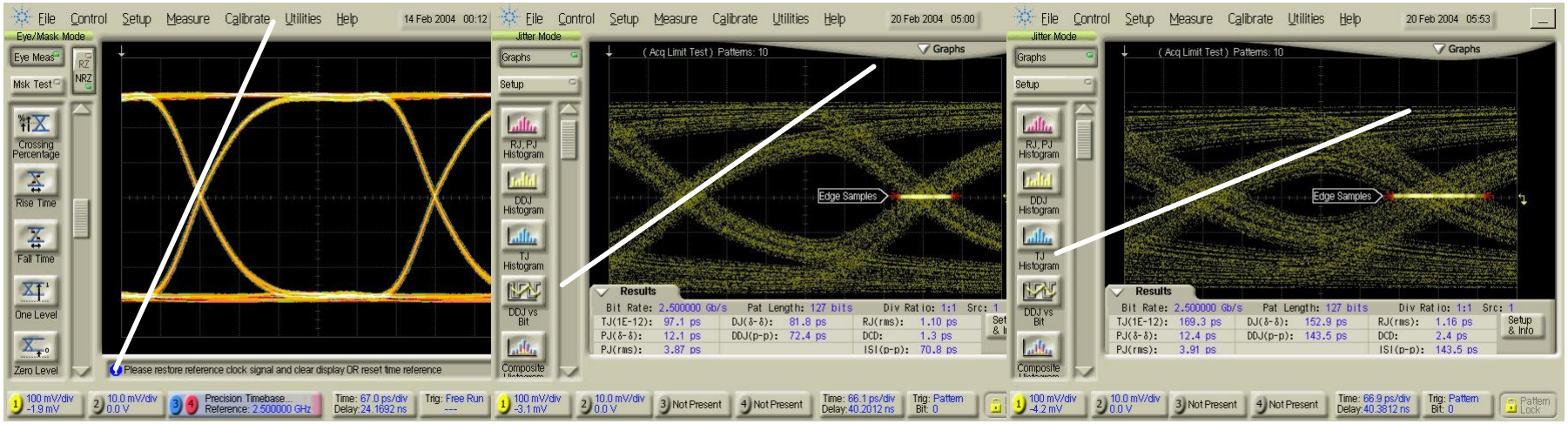
ISI changes rise/fall times

DDJ is caused by ISI∗DCD

ISI has both amplitude and timing components

→ changes the signal rise/fall times



Causes analyzer voltage noise to be mistaken for RJ

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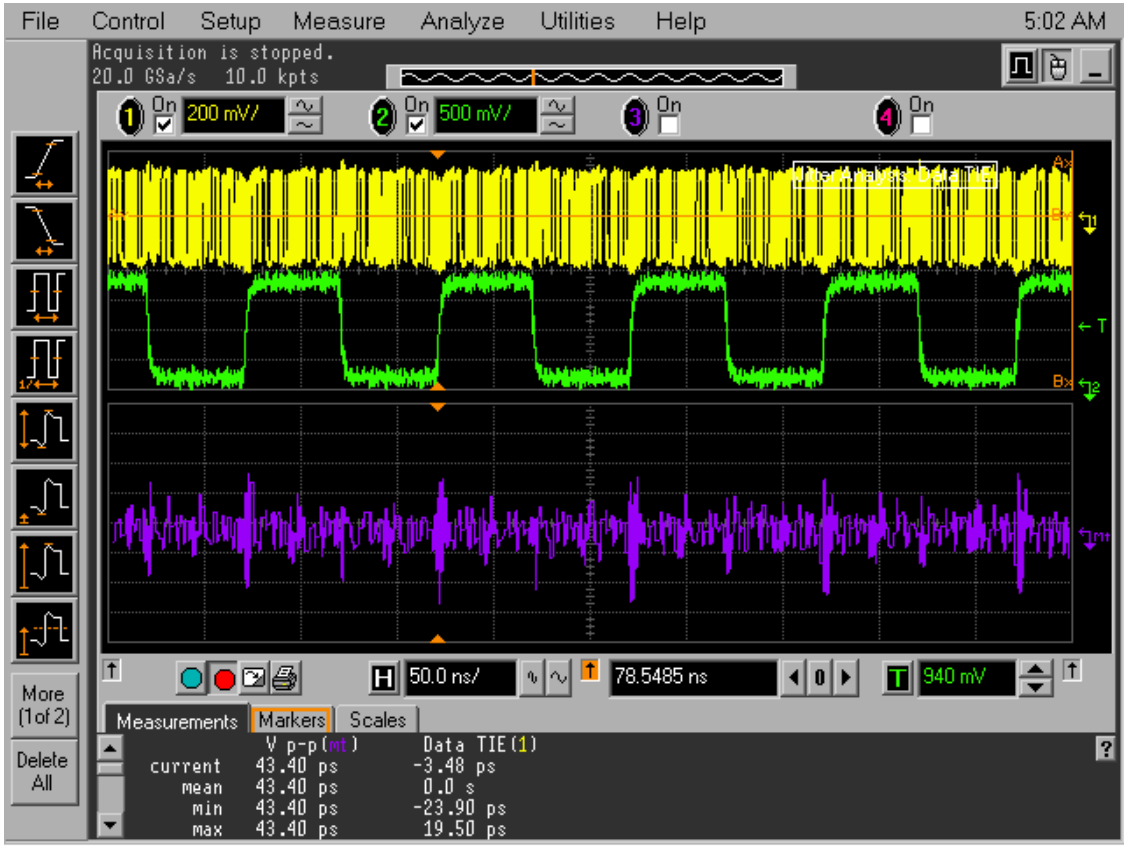
Uncorrelated Period Jitter Coupling



- **Trigger on "suspect" cross-talk coupling signals.**
- **Averaging Trend can help to eliminate RJ, ISI, & DCD and "draw-out" uncorrelated PJ component.**
- **With large uncorrelated PJ coupling component, you can sometimes identify corrupter using a Spectrum display without special triggering.**

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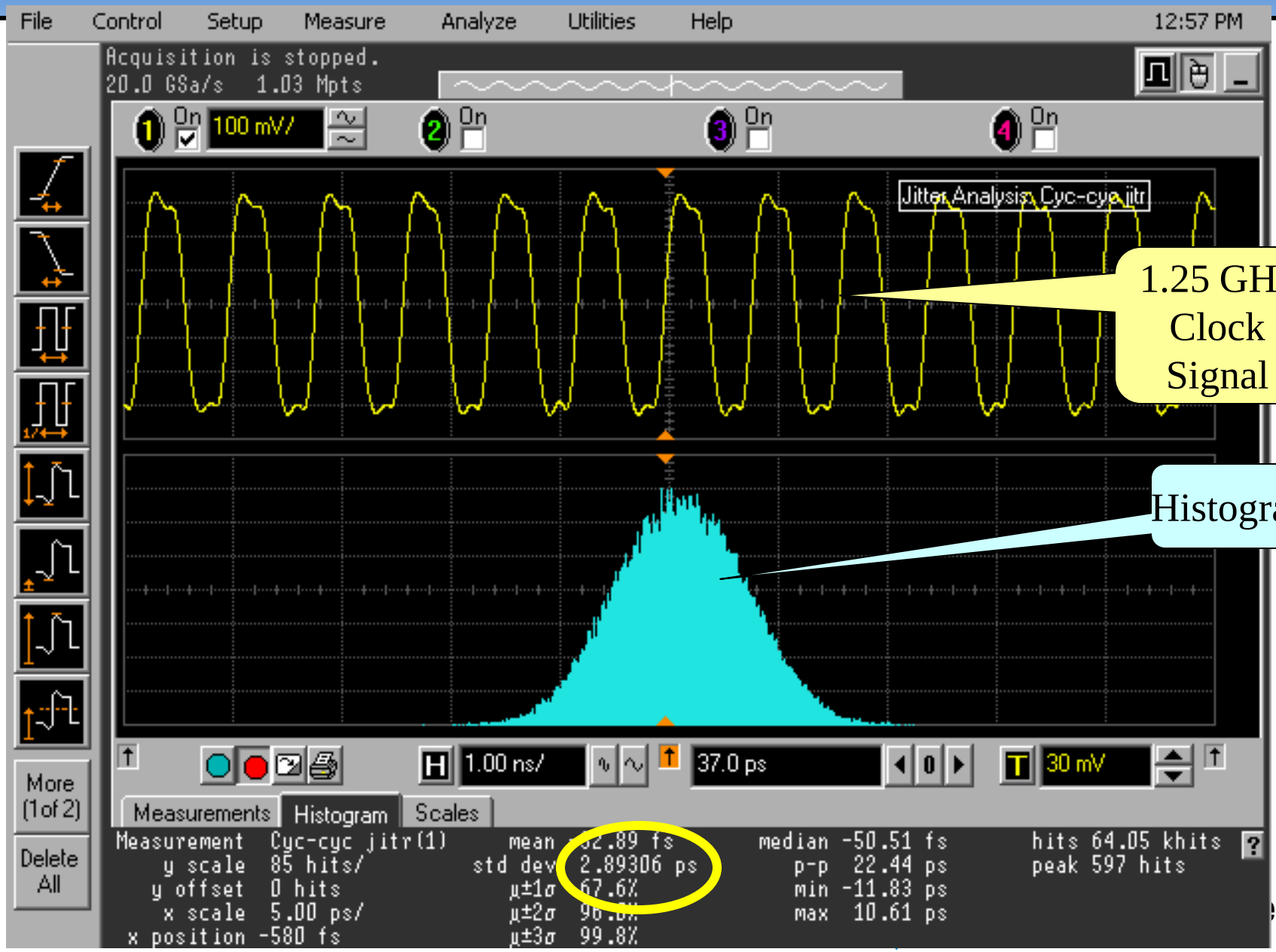
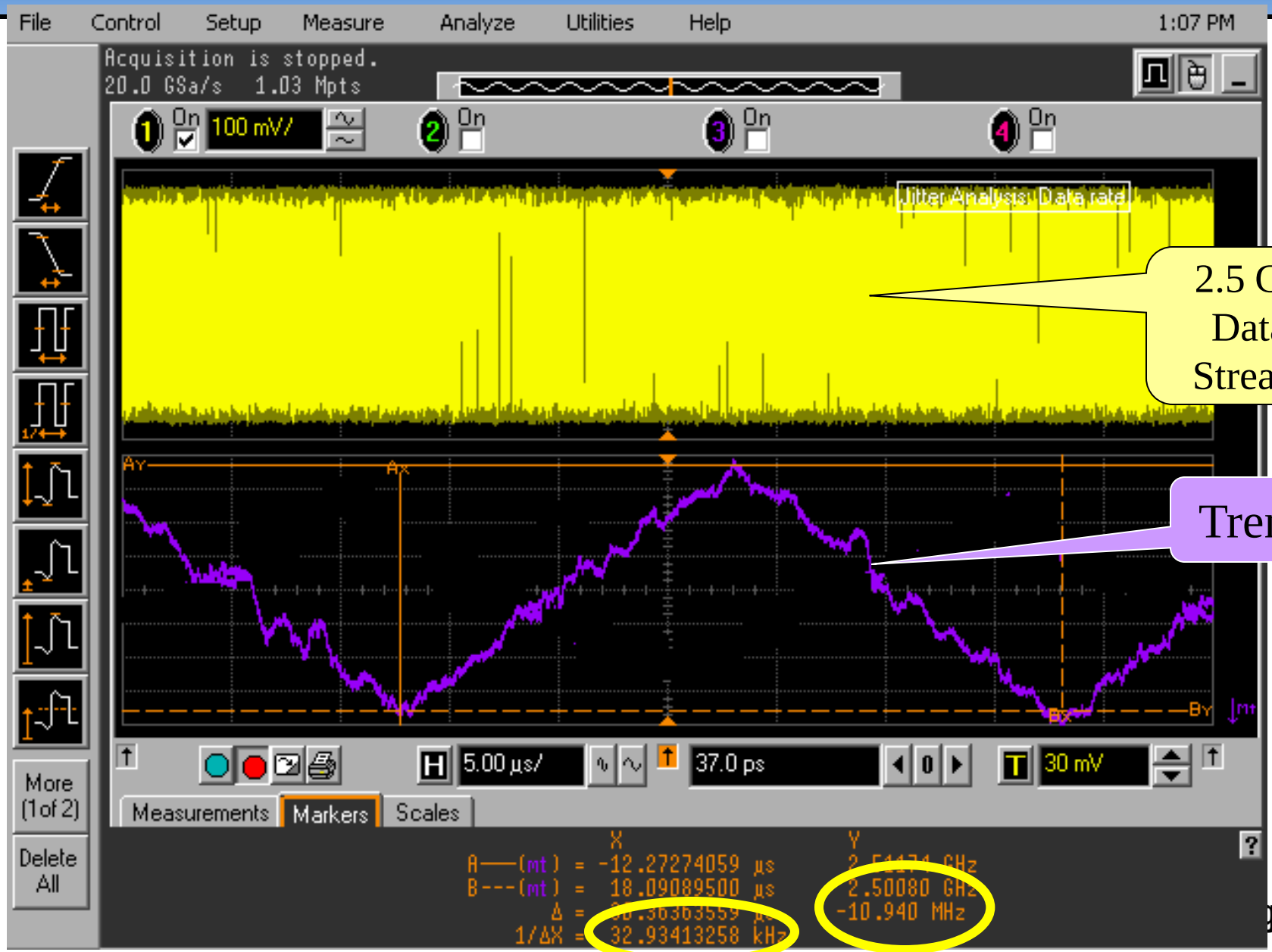
Cycle to Cycle Jitter Measurement



Spread Spectrum Clock Measurement



Random/Deterministic Jitter Separation

Jitter Breakdown helps focus on real issues

Advanced FFT Filtering and Signal Processing

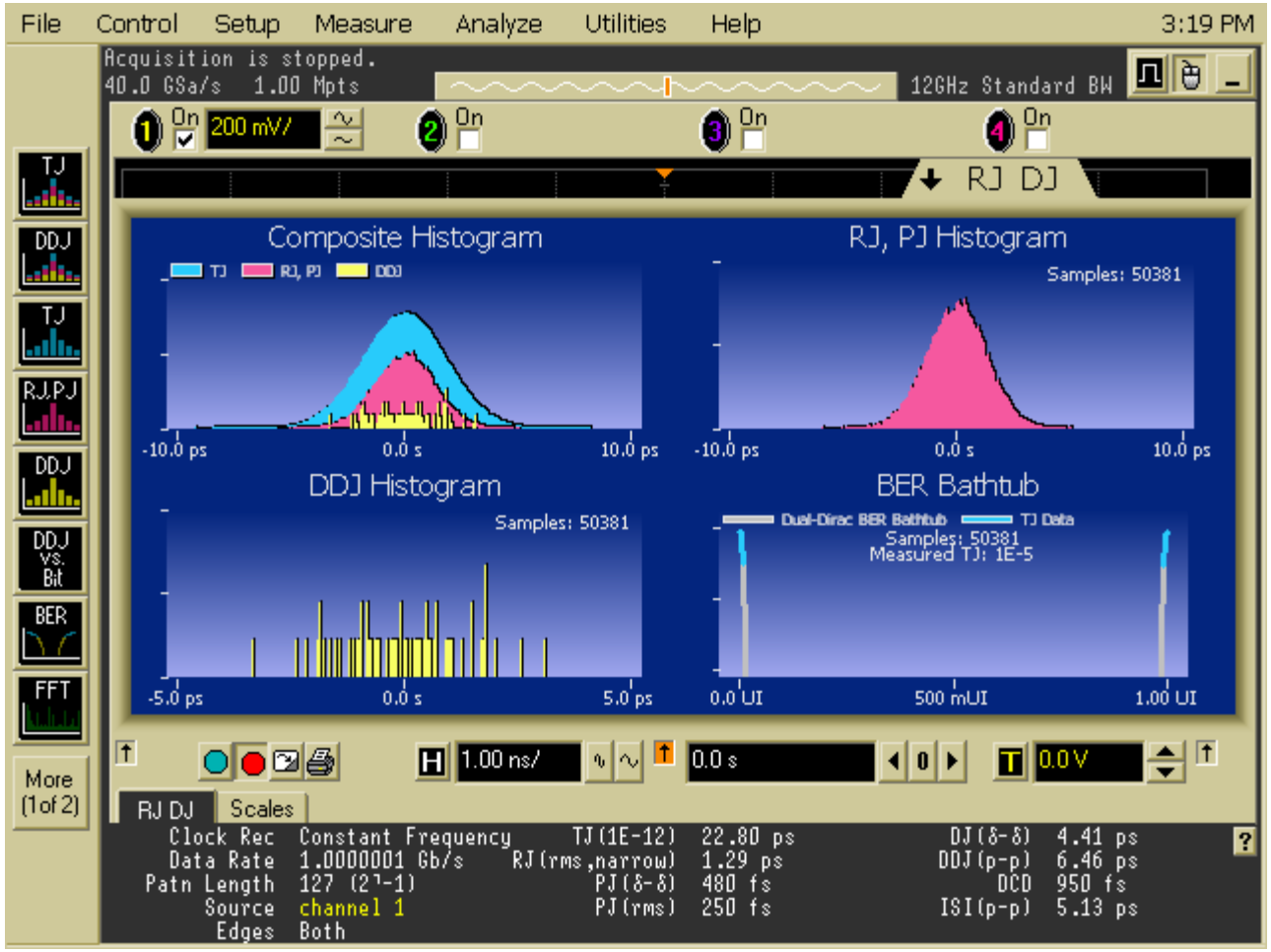
Decomposition of Deterministic Jitter and Random Jitter

Getting to the roots of the overall Jitter Deviatiation will help isolate

And Quantify the most significant Jitter contributors.

This will help Engineer to focus on the specific area of his design to improve the Jitter Value associated with it.

Base Case



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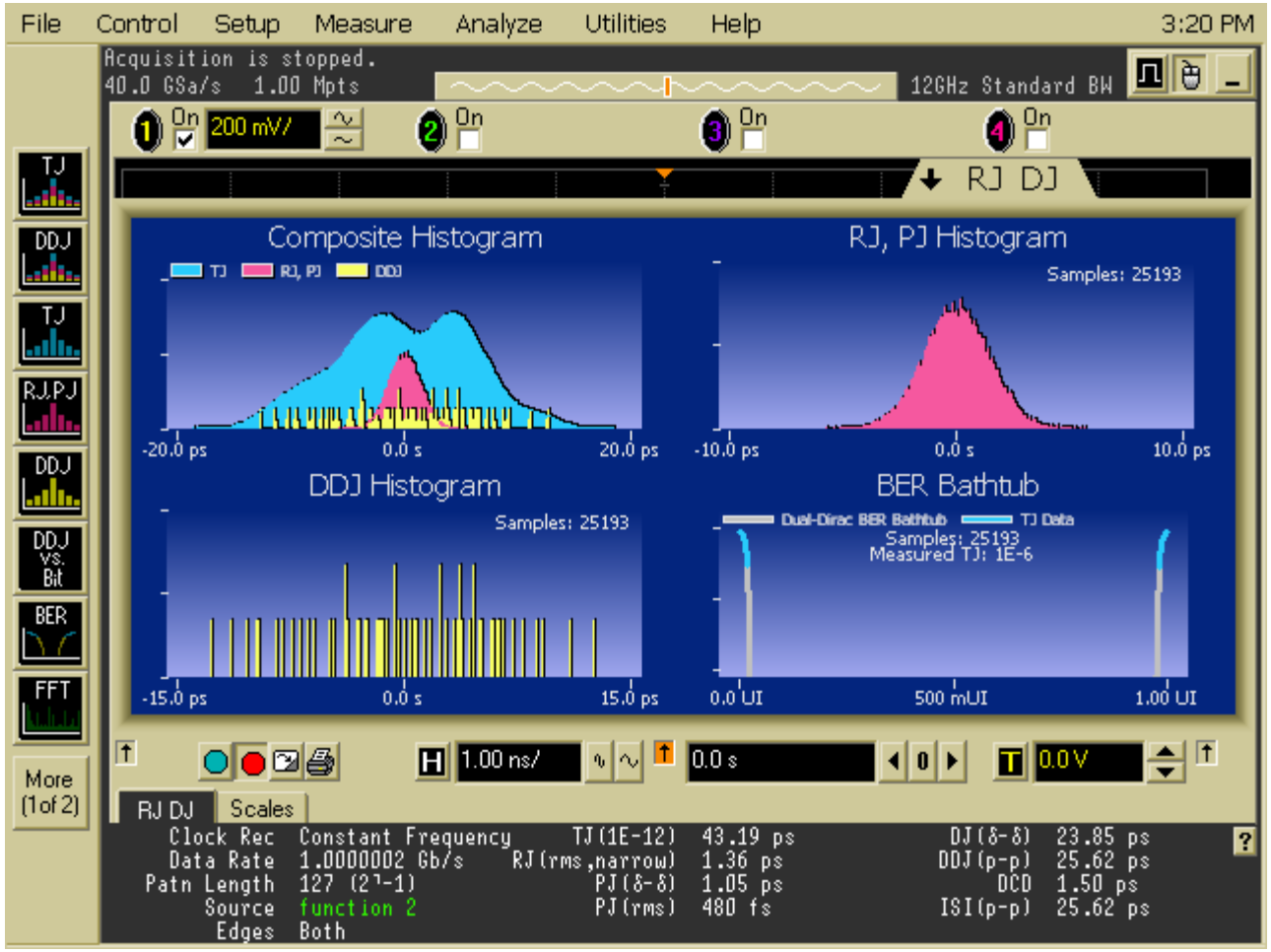
ISI Only



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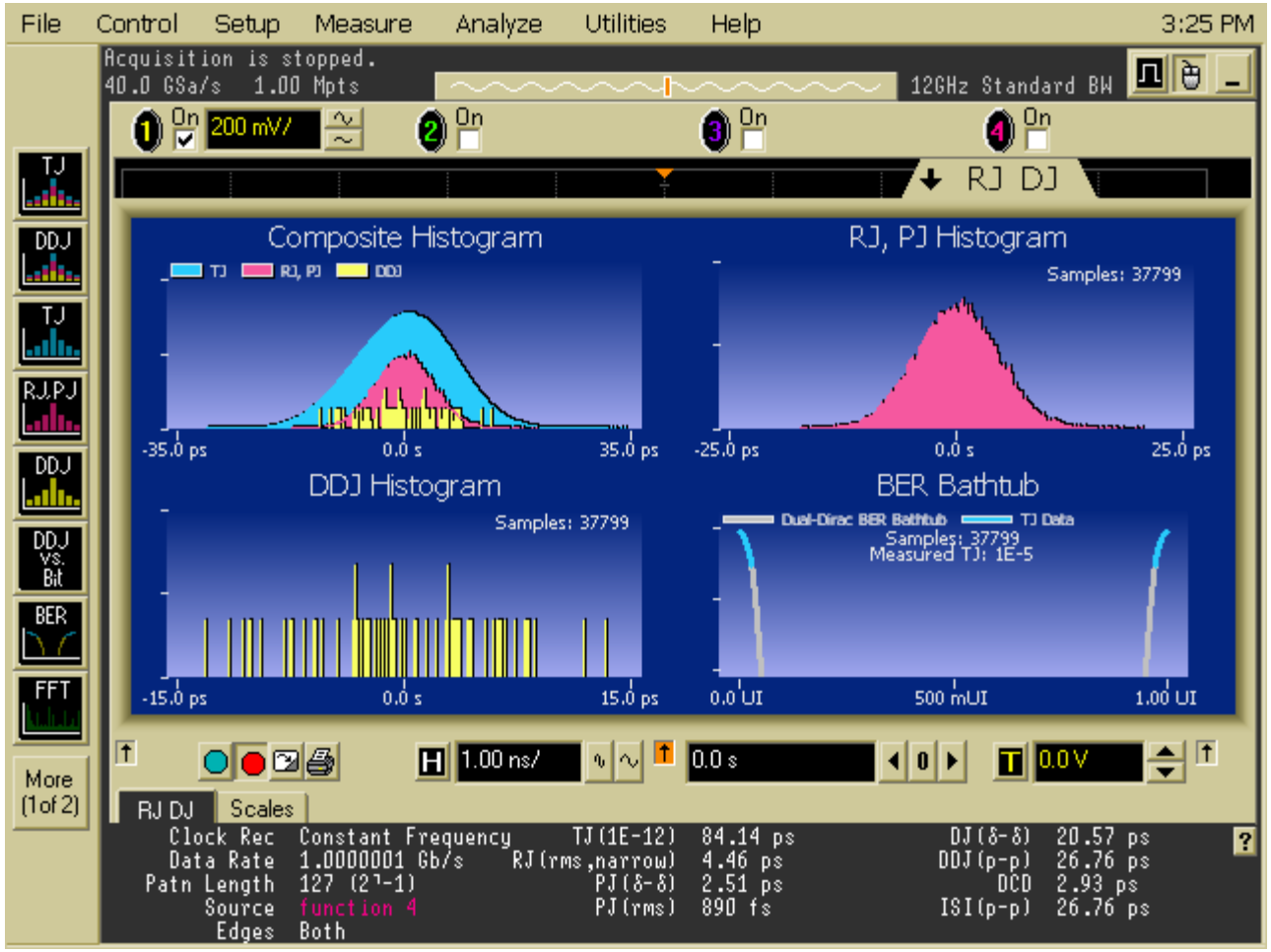
ISI and Random Jitter



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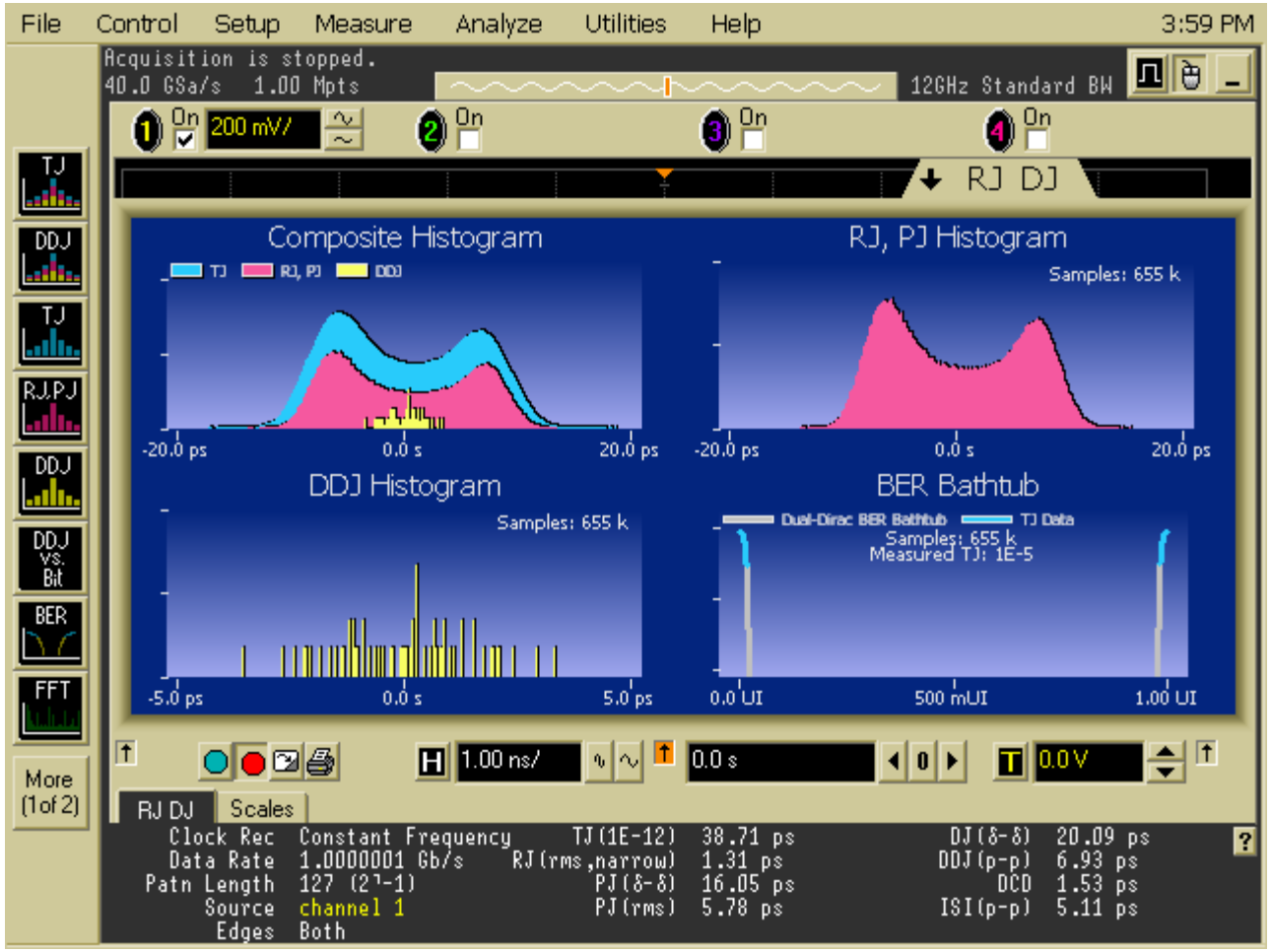
Adding Periodic Jitter

Pj Only



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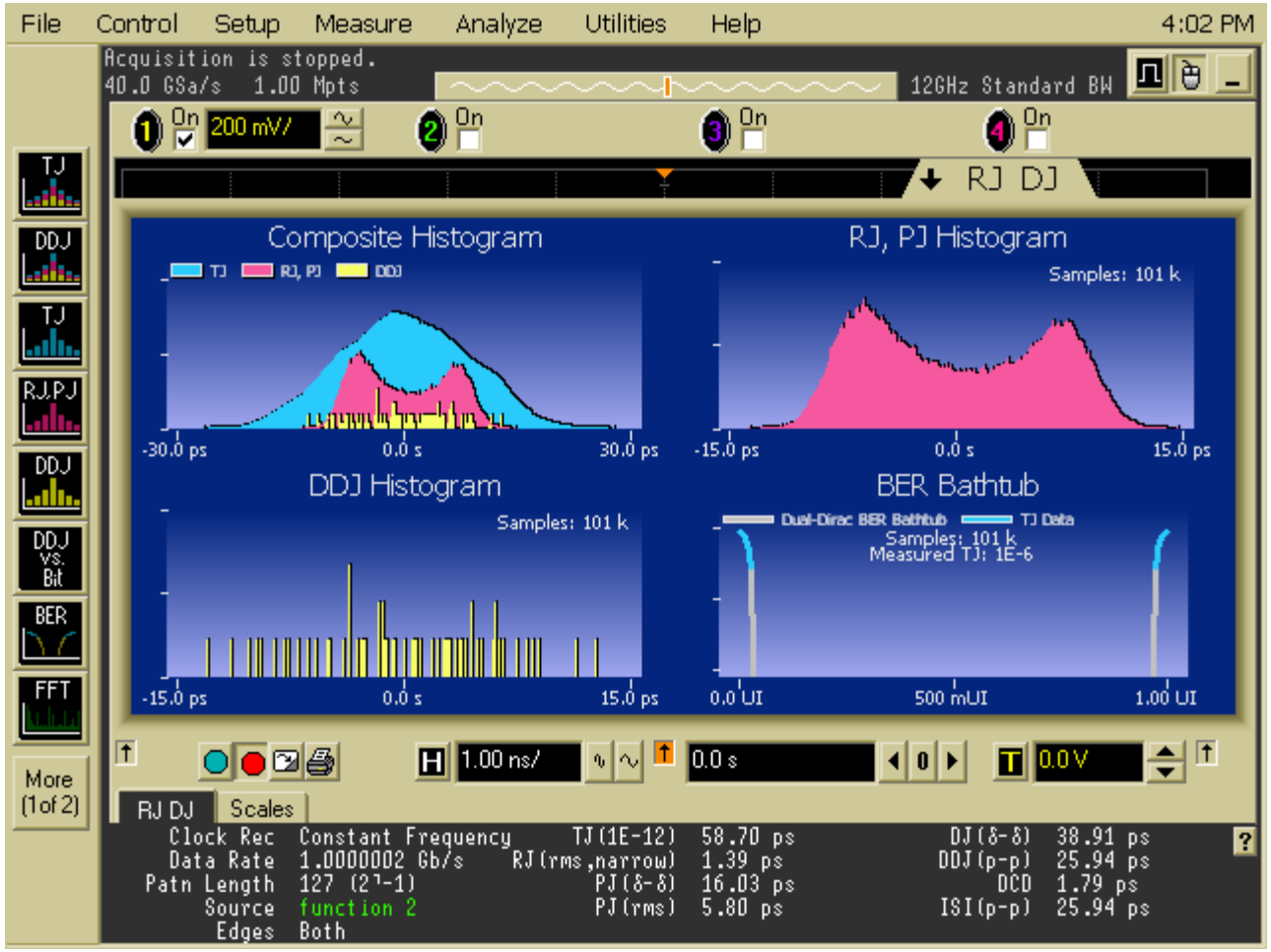
Pj + ISI



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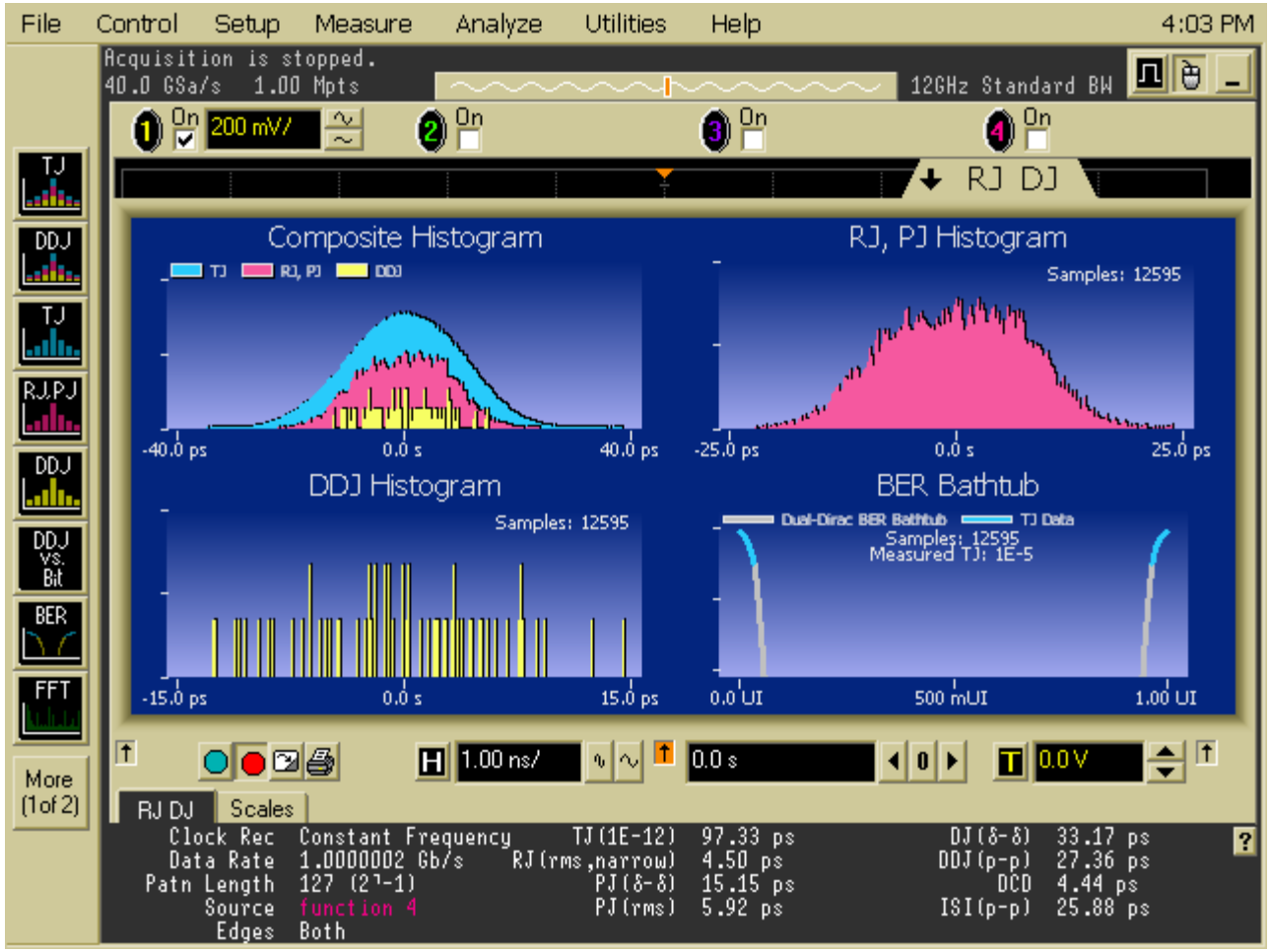
Pj + ISI + Rj



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How do we now Jitter Breakdown is accurate

A good question that if often asked about Jitter is:

How can we sure the Algorithms used in your Jitter Analysis Software are working accurately?

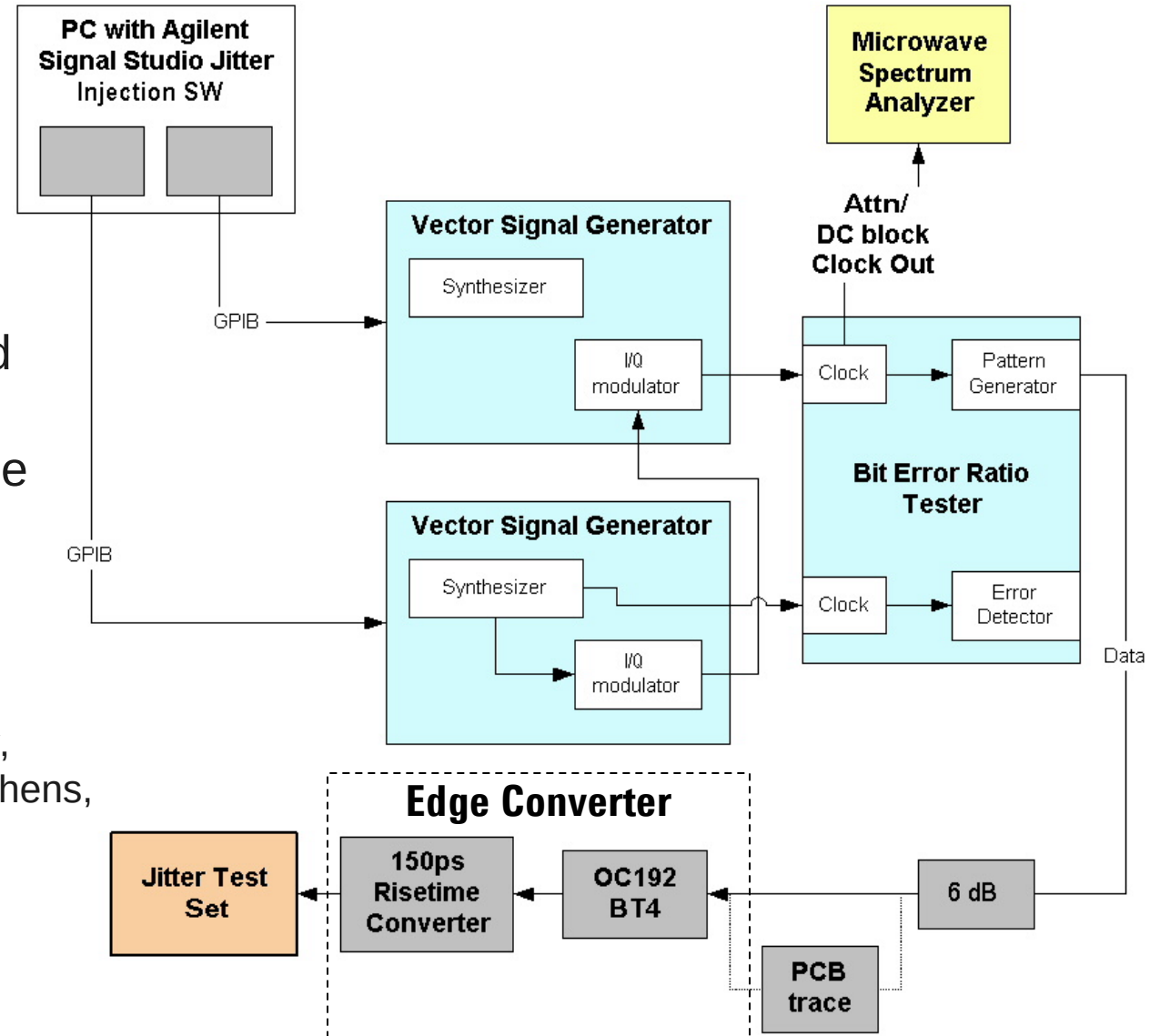
This a very good question and be confident we asked ourself this very question a long time ago when these Algorithms were initially developped for Telecom Applications on 86100 Equivalent Time oscilloscope.

The Answer is that we built a Precision Jitter Generator using only calibrated signal generators to try various signal Jitter conditions first individually then in combined cases.

The Precision Jitter Transmitter*

2.5 Gb/s
Single ended,
0.25 V levels
PRBS7 pattern

Calibration of applied jitter signals is traceable to reference standards



* Described in
Precision Jitter Transmitter,
Jim Stimple, Ransom Stephens,
DesignCon 2005

Available at
www.Agilent.com

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Enabling Debug, Characterisation and Compliance

In Addition to general purpose Jitter analysis tools, Agilent is member of several comitee to help define test methology and to provide comprehensive and exhaustive solution for the technologies of tomorrow

USB 2.0 3.0 / USB IF Wireles USB

HDMI 1.3

DISPLAYPORT

PCI EXPRESS 2.5Gb 5Gb 8Gb

SATA 1.5Gb 3Gb 6Gb

SAS 1.5Gb 3Gb

DigRF V3/V4

MIPI DSI/CSI